CHARACTERIZATION OF SURFACE STATES AT THE Si-SiO₂ INTERFACE

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I. INTRODUCTION

The present knowledge of thermally grown silicon dioxide layers is extremely broad. A lot of effort has been given in the past to understanding the Si-SiO₂ system, giving rise to the modern fabrication techniques for high quality LSI-circuits. Nevertheless, the exact physical nature of the Si-SiO₂ interface is still unresolved and many device characteristics still depend on poorly known properties of the thin interfacial layer between the silicon bulk and the amorphous silicon dioxide film. Surface generated leakage currents, 1/f-noise in MOSTransistors, carrier trapping and information losses in surface channel charge coupled devices are ascribed to so called "surface states" or "interface states".

Surface states are allowed energy levels in the forbidden energy gap located at the Si-SiO₂ interface. They can be donor or acceptor like. Occupied donor states are neutral, unoccupied donor states are positive, while acceptor states are negative when occupied and neutral when unoccupied. In the Si-SiO₂ system the

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interface states are mostly encountered as fast states, with time constants varying from a few nsec to tens of msec. The considerable dispersion in time constants at a fixed gate voltage can be explained by two different models. The tunneling model proposed by Preier accounts for the dispersion by a depth distribution over about 10 Angstroms yielding a broad range of tunneling time constants [1]. On the other hand, the surface potential fluctuation model of Nicollian and Goetzberger is based on oxide charge fluctuations [2].

The physical origin of surface states is located within a disordered region of a few atomic layers at the interface [3]. The defects responsible for the energy levels can be of an intrinsic nature, such as structural defects with dangling bonds [4], deficiency or excess of silicon or oxygen (Cheng [5], Johanessen and Spicer [6]). Extrinsic surface states are due to chemical impurities such as sodium or charged centers situated in the vicinity of the interface [7].

This paper describes some of the experimental techniques to assess the important electrical properties of interface states such as density, capture cross section and energy distribution. The classical high frequency C-V, low frequency C-V and conductance technique will be briefly reviewed. Charge pumping, deep level transient spectroscopy (DLTS), will be discussed. The weak inversion technique based on drain current measurements of MOS transistors in the weakly inverted region will be explained. Surface states characterization by means of 1/f-noise measurements of MOS transistors and by transfer loss experiments on surface channel charge coupled devices will also be discussed.

II. Metal-Insulator-Semiconductor Structure

For a detailed treatment on this subject we refer to the excellent handbooks of S. M. Sze [8], A. S. Grove [9], P. Cobbold [10]. The present review will be limited to those features of the C-V or G-V curves needed for the subsequent discussion on the experimental techniques. Although the derivation is valid for other kinds of MIS-systems, we refer to the Si-SiO$_2$ system.

Fig. 1 shows a MOS capacitor, consisting of a thin insulating SiO$_2$-layer on top of a p-type silicon substrate. $V_G$ is the voltage applied to the field plate and $t_{ox}$ is the thickness of the insulator which ranges from a few nanometers to several microns. A typical value for surface characterization is 100 nanometers.

The energy band diagram of the p-type semiconductor is shown in Fig. 2. Energy increases in a positive direction following the standard convention, the energy increases positively in Fig. 2