Chapter 8

Decoupling Power/Ground Planes

8.1 Introduction

It is likely that decoupling power and ground planes is one of the most misunderstood design concepts, and certainly the area having the most myths about the ‘correct’ decoupling strategy. The use of decoupling capacitors connected between the power and ground planes on a printed circuit board (PCB) is a common practice to help ensure proper functionality (i.e. signal integrity) and to reduce EMI emissions from printed circuit boards. The proper number and value of decoupling capacitors is always a topic of debate between EMC engineers and design engineers. Some typical rules-of-thumb include requiring a decoupling capacitor for each power pin on an IC, at least one decoupling capacitor per side of physically large ICs, and/or decoupling capacitors spread evenly over every square inch of the board. Few qualitatively proven approaches for the optimal approach to decoupling is available in the technical literature. These rules-of-thumb can often result in drastic over-design of the decoupling strategy, since the saying ‘better safe than sorry’ is often applied. Many of these rules are really based in myth. In addition, there are a number of outright myths that exist and are published, causing significant confusion within the general design community. Some of these myths have some level of rationale justifying them; others do not. One published article claimed that the decoupling capacitors actually caused the emissions! Unfortunately, many myths seem infinitely plausible and are not easy to discount.
Traditionally, the values of the decoupling capacitors are largely based upon habit and the experience of the EMC engineer. Values of 0.01 uF or 0.1 uF are typically used. Often smaller capacitors are used in parallel with the main decoupling capacitor to provide a high-frequency and a low-frequency filtering effect. By using multiple capacitor values in close proximity, however, there is a risk of causing cross resonances that can have an adverse effect on noise and emission levels.

The overall result is that a design approach for the power plane decoupling (between a power plane and a ground reference plane) has historically been difficult to develop or analyze. With on-board clock speeds of 400 – 800 MHz becoming common, a more rational approach must be taken to optimize the design of decoupling capacitors on the printed circuit (PC) board.

8.2 Background

There are two primary purposes for using decoupling between power and ground-reference planes. The first purpose is for functionality, that is, the decoupling capacitor is a charge storage device, and when the IC switches state and requires additional current, the local decoupling capacitor supplies this current through a low inductance path. If the capacitor is able to supply all of the current required by the IC, then the voltage at the IC power pin remains constant at the desired supply voltage. If the capacitor is not able to supply the required current, then the voltage at the IC power pin is lowered temporarily until adequate current is provided, or until the need for the current is ended. If sufficient current is not provided, the IC may experience a functional failure. It is important, therefore, to locate decoupling capacitors close to the demand for current (IC power pins). It is also important to provide a low impedance path from the IC power pins to the power plane, from the IC’s ground-reference pins to the ground-reference plane, and from the decoupling capacitor to the power and ground-reference planes. Capacitors used for this charge delivery function must have low equivalent series resistance (ESR) and low equivalent series inductance (ESL). Table 8-1 shows typical values for different SMT capacitor types.