Chapter 5

FOLDING/INTERPOLATING ADCS

Analog Preprocessing Techniques for High-Speed 8-bit ADC

Koen Uyttenhove, J. Vandenbussche, G. Gielen and M. Steyaert

Abstract Designing high-speed flash ADCs in a deep submicron technology requires optimized architectures and building blocks. In this chapter, the design of a high-speed 8-bit converter is presented, following the discussion of analog pre-processing techniques necessary to reduce the power consumption and input capacitance of the converter. Three analog preprocessing techniques will be described, two of which will be used in the design of the 8-bit converter. The systematic design of an 8-bit interpolating/averaging converter will then be described and experimental results will be presented.

5.1 INTRODUCTION

Analog preprocessing techniques are necessary to reduce the power consumption of future high-speed analog to digital converters (ADC). In this chapter two of these techniques are used to implement a high-speed 8-bit, 200-MSample/s ADC. After a general introduction on the different preprocessing techniques used in the design of high-speed analog to digital converters, the systematic design of a high-speed, high-accuracy Nyquist-rate A/D converter will be proposed. The presented design methodology covers the complete flow and is supported by software tools. A generic behavioral model is used to explore the A/D converter’s specifications during high-level system design and exploration. The inputs to the cooonverter design are the specs of the A/D converter and the technology process. The result is a generated layout and the corresponding extracted behavioral model. The approach has been applied to a real-life test case, where a Nyquist-rate 8-bit 200 MS/s 4-2 interpolating/averaging A/D converter was developed.

5.2 ANALOG PREPROCESSING TECHNIQUES IN ADCs

Flash architectures are typically the simplest and the fastest structures that can be used to implement analog to digital converters. Figure 5.1 presents a block diagram of a N-bit flash converter. The resistive ladder subdivides the converter reference...
voltage \((+V_{\text{ref}} - V_{\text{ref}})\) in a set of \(2^N\) reference voltages, which are compared in parallel with the analog input signal. A logic decoder converts the thermometer code generated by all the comparators into a binary code that approximates the input signal every clock cycle.

Note that the major advantages (simplicity and parallelism) of flash architectures also present its main problem: the number of comparators increases exponentially with the resolution specification, leading typically to a large die area and a high power consumption. Normally, this architecture is only used to implement converters with a resolution less than about 6 bit. Also, the large input capacitance limits the use of this structure for high-speed converters with resolutions above 6 bit.

Therefore, three preprocessing techniques are used in the area of high-speed converters with a resolution of 8 bits and more [Raz 95]:

- Folding techniques
- Interpolating techniques
- Averaging techniques

These three techniques will now be discussed in more detail whereby their advantages and disadvantages will be pointed out.

### 5.2.1 Folding techniques

Folding is a preprocessing technique, used to reduce the number of comparators in a high-speed ADC. By doing this, power consumption can be decreased [Ven 96]. The folding technique consists in subdividing the input-output characteristic of a typical flash architecture into several parts of equal length which are folded.