Chapter 3

High-speed A/D converters

3.1 Introduction

The best-known architecture for a high-speed analog-to-digital converter is the flash converter structure. In this structure an array of comparators compares the input voltage with a set of increasing reference voltages. The comparator outputs represent the input signal in a digital (thermometer) code which can be easily converted into a Gray or binary weighted output code. The flash architecture shows a good speed performance and can easily be implemented in an integrated circuit as a repetition of simple comparator blocks and a (ROM) decoder structure. However, this architecture requires $2^N-1$ comparators to achieve an $N$-bit resolution. The parallel structure makes it difficult to obtain a high-resolution while maintaining at the same time a large bandwidth, a low power consumption, and a small die size.

Interpolation between reference levels reduces the number of reference taps and input amplifiers resulting in a lower power consumption. The influence of offset voltages in the input amplifiers can be reduced by using averaging between active amplifier stages. At the same time, signal-to-noise ratio is improved without using more power. An alternative to the full-flash architecture is the multi-step A/D conversion or sub ranging principle. In high-speed converters the two-step architecture is the most popular because of the ease of implementation. However, a two-step architecture must be preceded by a sample-and-hold amplifier which performs the sampling of the analog input signal. In the two-step architecture a coarse and fine quantization takes place. These succeeding conversion steps need time. The sample-and-hold operation on the signal keeps the sampled signal constant. During this “hold” time the conversion takes place, making it virtually “timeless.” Af-
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After the coarse quantization is performed, the digital signal is applied to a D/A converter to reconstruct the analog signal. This reconstructed signal is subtracted from the analog input signal which is held by the sample-and-hold amplifier. After subtraction has taken place the residue signal can be amplified and is then applied to the fine quantizer which performs the conversion into a digital value. The coarse plus fine output code with, in many cases, an error correction operation results in the final digital output word. A good balance between circuit complexity, power consumption, and die size is obtained in this type of converter. The final dynamic performance, however, depends substantially on the quality and dynamic performance of the sample-and-hold amplifier.

In MOS technology circuits can be operated in a continuous-time mode or in a discrete-time mode. Most architectures in MOS use a discrete-time mode of operation. In such a solution the sample-and-hold operation is combined with the system function. Mostly the discrete-time operation includes an automatic offset cancelation technique in the comparator stages. In a full-flash system, $2^N - 1$ small sample-and-hold amplifier-comparators are therefore used to perform the conversion function. Because of the small value of the hold capacitor, offsets induced by switching transients and channel charges of the switching devices limit the resolution of the total system.

In MOS using a discrete-time circuit solution a two-step system implementation can be easily obtained by using a set of coarse sampled data comparator-amplifiers stages and a set of identical fine stages. The coarse conversion is performed by comparing the input signal with the coarse tap voltages on the input ladder. After the coarse value is determined, a block of fine reference voltages is switched on. These reference voltages are in-between the two already determined coarse ladder taps. Again a comparison is performed and the final output code is obtained. In this system the ladder is used for coarse and fine quantization without needing an extra D/A subtracter circuit to drive the fine converter stage.

Pipeline converter architectures are very popular in CMOS technology. This architecture consists of a cascade of simple modular converter blocks performing between 1 and 5 bit conversions each. Each block consists of an A/D converter, a D/A converter for the reconstruction of the analog signal, a subtracter to determine the signal residue after the quantization and a gain stage. A sample-and-hold function is part of the converter block. Analog data is delayed by the sample-and-hold amplifier stage during the conversion resulting in an output code latency equal to the number of cascaded stages.