Chapter 7

Sample-and-hold amplifiers

7.1 Introduction

In this Chapter sample-and-hold amplifiers are discussed. In most cases practical implementations of these amplifiers are track-and-hold amplifiers. During the sampling mode the input signal is "tracked" and a sample is taken at the moment the system is switched into the hold mode. A sample-and-hold amplifier samples the analog input signal during a short time and then holds the signal during the full clock period giving the analog-to-digital converter about twice the time to perform the conversion as in the case of a track-and-hold amplifier.

The terminology sample-and-hold amplifier will be used in this chapter although most systems are track-and-hold amplifiers.

A sample-and-hold amplifier is a crucial part in a high-speed or high-resolution A/D converter system. Using a very simple model of a sample-and-hold amplifier, a number of specifications will be analyzed and the optimum switch configuration will be defined. Next, different circuit configuration options for sample-and-hold amplifiers will be discussed. An important factor is charge feed-through when a sample-and-hold amplifier is switched from the track mode (or sample mode) into the hold mode. Furthermore, this charge feed-through must be signal level independent to avoid distortion. Single ended circuit implementations are limited by charge feed-through. An optimum circuit configuration is obtained with a differential system implementation. Overall A/D converter system performance, such as dynamic range, distortion, SFDR, and noise, are largely dependent on the sample-and-hold
amplifier. Examples of single ended and differential sample-and-hold circuits will be discussed. In submicron CMOS technology the supply voltage is reduced to about 1 V. This reduction in supply voltage has significant influence on the switching performance of PMOS or NMOS switches. Especially when switches are bias around half the supply voltage, then the on resistance will become large. This is not allowed because of the large distortion and noise such a switch introduces. To overcome this problem, clock bootstrapping with high voltage MOS devices is used for the switches. Different system implementations will be discussed. Furthermore a distortion analysis is given showing the influence of the rise or fall time of the sampling clock when a single MOS device is used as a sampling switch. Separate designs of sample-and-hold amplifiers are very limited described in literature. Mostly the S/H amplifier is part of a converter design and many times even there the description of this functional block is very limited.

7.2 Basic sample-and-hold configuration

The simplest form of a non-inverting sample-and-hold circuit consists of a switch $S$ with ON resistance $R_s$ and the hold capacitor $C_H$. At the input of the circuit a voltage source $V_{in}$ is applied. A circuit with basically an infinite input impedance must be used to sense the output voltage $V_{out}$ available across the hold capacitor. In this simple system this "hold" mode amplifier is not shown. The information is stored as charge on the capacitor $C_H$. To avoid voltage droop a low leakage capacitor must be used with a small dielectric adsorption. The dielectric adsorption can result in voltage changes during the hold mode. As an example, a fully discharged capacitor may still show a voltage across the terminals after the short circuit switch, used to discharge the capacitor, is opened. The basic system is shown in Figure 7.1. This simple circuit can be used to determine some of the most important limitations of a sample-and-hold system.

7.2.1 Signal bandwidth

The small signal bandwidth of the system is determined by the ON resistance of the switch $R_s$ optionally enlarged with the output impedance of the signal source driving this system. We obtain for the small signal bandwidth:

$$f_{-3\,dB} = \frac{1}{2\pi R_s C_H}.$$  \hspace{1cm} (7.1)