Chapter 4

Placement

4.1 Introduction

This chapter addresses the placement problem for high-performance analog circuits. The placement phase is crucial for the performance degradation of an analog circuit layout since it influences all the parasitic layout effects which have been discussed in chapter 2. The distance between matching devices, and therefore also their matching degree is determined during placement. The placement of a circuit also determines its thermal profile. In addition, it greatly influences the values of the interconnect parasitics. Although their final values are determined during routing, their minimum values are fixed by the configuration of the device terminals, which is determined during placement. A performance driven placement algorithm therefore has to take into account all of these performance degrading effects simultaneously.

We begin this chapter by formally stating the problem and reviewing the constraints that have to be taken into account during placement. We then give a brief overview of our placement tool in section 4.3. In order to justify our choice of simulated annealing as basic placement optimization algorithm, we give an overview and comparison of different placement techniques in section 4.4. Based on this comparison, the simulated annealing algorithm is selected and its application to analog performance driven placement is discussed in section 4.5. Some important details of our placement implementation, the placement model, the handling of analog constraints, the move set and cost function are discussed in sections 4.5.1, 4.7 and 4.8. In section 4.9 we describe in detail how the layout induced performance degradation is computed for an intermediate placement solution. In section 4.11 we discuss the annealing schedule of the algorithm. Finally, we give some experimental results in section 4.12 and we draw conclusions in section 4.13.

4.2 Problem Formulation

The analog circuit level placement problem can be stated as follows: given an electrical circuit specified as a set of devices (transistors, capacitors and resistors) and a netlist interconnecting terminals on these devices and on the periphery of the circuit itself, select an optimal implementation (variant) for each device, and position these variants on the layout surface in a design rule
correct way and such that the layout area is minimal and that the circuit can be routed afterwards. The following additional constraints and objectives have to be added to this basic definition:

- **Symmetry Constraints**
  
  In high-performance analog circuits, it is often required that groups of devices are placed symmetrically with respect to one or more symmetry axes. Symmetric placement allows for symmetric routing and results in matched parasitics. Symmetry constraints can be formulated in terms of *couples, self-symmetric devices* and *symmetry groups*. Two devices which are placed symmetrically with respect to an axis form a couple. A self-symmetric device is a device which is placed on a symmetry axis. A symmetry group is a collection of couples and self-symmetric devices which share the same symmetry axis. The symmetry group represented in Fig. 4.1 consists of the couples (M1A,M1B) and (M2A,M2B) and the self-symmetric device M5. More than one symmetry group can be specified for a circuit. The presence of one or more symmetry groups has the following implications for analog placement:

  - Two devices which are specified as a couple must be placed symmetrically with respect to an axis and must have identical variants and mirrored orientations.
  - A device which is specified as self-symmetric must be placed on a symmetry axis.
  - Couples and self-symmetric devices that belong to the same symmetry group must share the same symmetry axis.

- **Matching Constraints**
  
  Matching constraints can be specified by defining matching groups. A matching group is a set of two or more devices for which an accurate ratio of device characteristics is required. The simplest and most common case of a matching group is a pair of equal devices. A more complicated case of a matching group is shown in Fig. 4.2. Any number of matching groups can be defined in an analog circuit. The presence of one or more matching groups has the following implications for analog placement:

  - All devices which belong to the same matching group must have equal orientations.
  - If the devices of a matching group are equal (1:1 ratios), they must be implemented with equal variants. If they have another ratio, they should be built of equal unit devices, according to the ratio.
  - The placement tool has to determine the positions and therefore also the distance between the matched devices such that the circuit performance constraints are met. Since it is not always possible in an analog circuit layout to, at the same time, meet all symmetry requirements, put all matching devices directly next to each other and obtain a fairly compact layout, the matching degree of a pair of devices has to be selected in view of its influence on the performance of the circuit.