Chapter 3

CMOS D/A Converter Architectures

3.1 Introduction

In the previous chapter, the functionality of a D/A converter has been explained together with the specifications that describe its static and dynamic behaviour. This chapter discusses the different architectures for a D/A converter.

A D/A converter generates for each digital input code a multiple of a certain reference quantity. Dependent on this quantity (a voltage, a charge or a current), three classes of D/A converters can be identified namely the resistor, the capacitor and the current steering architecture. In the first part of this chapter, both the resistor and the capacitor D/A converter will be discussed. It is the intention of the author to emphasise the existence of these architectures as useful alternatives for the current steering architecture. For a detailed study the reader is referred to [Razavi, Johns]. The remainder of this chapter describes the current steering topology. Three possible implementations together with their advantages and disadvantages will be discussed in detail. During the remainder of this thesis, this architecture will be analysed with regard to its static and dynamic performance.

3.2 The Resistor D/A Converter

3.2.1 The resistor string D/A converter

In this type of D/A converter, a reference voltage is divided into $2^N - 1$ parts by selecting one tap of a segmented resistor string using a switching network (fig.3.1). Although this implementation provides a simple and inherently monotonic D/A conversion, it has some major drawbacks. For resolutions higher than eight bits, the
occupied silicon area becomes fairly large. For a ten bit D/A converter, 1023 resistors and 1024 switches are required. Furthermore, the delay through the switching network poses a severe limitation on the update rate of the D/A converter.

The integral non linearity error is directly related to the matching precision of the used resistors. Due to uncertainties during processing, the values of the resistors in the resistor string will not be equal. The relative mismatch between two resistors is given by:

$$\frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} + \frac{\Delta L}{L} - \frac{\Delta W}{W} - \frac{\Delta t}{t} + \frac{\Delta R_C}{R} \quad (3.1)$$

with $R_C$ the contact resistance, $L$ the length, $W$ the width, $t$ the thickness and $\rho$ the resistivity of the resistor. The width, length and value of the resistor can be freely chosen by the designer as to minimise the mismatch. However, larger dimensions need more silicon area and create a higher capacitance to the substrate.

The influence of this mismatch on the integral non-linearity error of the resistor string D/A converter is given by [Razavi]:

$$INL = \frac{V_{ref}}{\sqrt{4N}} \frac{\Delta R}{R} \quad (3.2)$$

which is reached at the middle of the resistor string. Since this formula is a standard deviation, it has to be interpreted as follows. In 68 % of the cases, the non-linearity error will be smaller than or equal to the value calculated in eq.(3.2).

For high speed, high accuracy applications, this architecture is no longer the preferred solution.