Chapter 1

Introduction to SystemVerilog

This chapter provides an overview of SystemVerilog. The topics presented in this chapter include:

- The origins of SystemVerilog
- Technical donations that went into SystemVerilog
- Highlights of key SystemVerilog features

1.1 SystemVerilog origins

SystemVerilog is a standard set of extensions to the IEEE Std. 1364-2001 Verilog Standard (commonly referred to as "Verilog-2001"). The SystemVerilog extensions to the Verilog HDL that are described in this book are targeted at design and writing synthesizable models. These extensions integrate many of the best features of the SUPERLOG and C languages. SystemVerilog also contains a large number of extensions targeted toward verification of large designs. These verification extensions integrate features from the SUPERLOG, VERA C, C++, and VHDL languages, along with OVA assertions and PSL assertions (formerly known as Sugar). These verification assertions are in a forthcoming companion book, SystemVerilog for Verification.
This integrated whole created by SystemVerilog greatly exceeds the sum of its individual components, creating a new type of engineering language, a Hardware Description and Verification Language or HDVL. Using a single, unified language enables engineers to model large, complex designs, and verify that these designs are functionally correct.

The SystemVerilog enhancements are being defined by a standards group under the auspices of the Accellera Standards Organization, rather than directly by the IEEE. Accellera's stated goal is to turn the definition of SystemVerilog over to the IEEE for ratification as part of the full IEEE 1364 standard. It is expected that SystemVerilog will be a major portion of the next generation of the Verilog standard.

The Accellera standards organization

Accellera is a non-profit organization with the goal of supporting the development and use of Electronic Design Automation (EDA) languages. Accellera is he combined VHDL International and Open Verilog International organizations. Accellera helps sponsor the IEEE 1076 VHDL and IEEE 1364 Verilog standards groups. In addition, Accellera sponsors a number of committees doing research on future languages. SystemVerilog is the result of one of those Accellera committees. Accellera itself receives its funding from member companies. These companies comprise several major EDA software vendors and several major electronic design corporations. More information on Accellera, its members, and its current projects can be found at www.accellera.org.

SystemVerilog is based on proven technologies. Various companies have donated technology to Accellera, which has then been carefully reviewed and integrated into SystemVerilog. A major benefit of using donations of technologies is that the SystemVerilog enhancements have already been proven to work and accomplish the objective of modeling and verifying much larger designs.

1.1.1 The Accellera SystemVerilog standard

Accellera has based the SystemVerilog enhancements to Verilog on proven technologies. Various companies have donated technology to Accellera, which has then been carefully reviewed and integrated into SystemVerilog. A major benefit of using donations of technologies is that the SystemVerilog enhancements have already been proven to work and accomplish the objective of modeling and verifying much larger designs.

A major portion of SystemVerilog was released as an Accellera standard in June of 2002 under the title of SystemVerilog 3.0. This initial release of the SystemVerilog standard allowed EDA compa-