A Fully Fault-Tolerant Representation of Quantum Circuits

Alexandru Paler\textsuperscript{1}, Ilia Polian\textsuperscript{1}, Kae Nemoto\textsuperscript{4}, and Simon J. Devitt\textsuperscript{2,3,4}

\textsuperscript{1} University of Passau, Innstr. 43, 94032 Passau, Germany
alexandru.paler@uni-passau.de
\textsuperscript{2} Ochanomizu University, 2-1-1 Ottsuka, Bunkyo-ku, Tokyo 112-8610, Japan
\textsuperscript{3} Graduate School of Media and Governance, Keio University, Fujisawa, Kanagawa 252-0882, Japan
\textsuperscript{4} National Institute of Informatics, 2-1-2 Hitotsubashi, Chiyoda-ku, Tokyo, Japan

Abstract. We present a quantum circuit representation consisting entirely of qubit initialisations (I), a network of controlled-NOT gates (C) and measurements with respect to different bases (M). The ICM representation is useful for optimisation of quantum circuits that include teleportation, which is required for fault-tolerant, error corrected quantum computation. The non-deterministic nature of teleportation necessitates the conditional introduction of corrective quantum gates and additional ancillae during circuit execution. Therefore, the standard optimisation objectives, gate count and number of wires, are not well-defined for general teleportation-based circuits. The transformation of a circuit into the ICM representation provides a canonical form for an exact fault-tolerant, error corrected circuit needed for optimisation prior to the final implementation in a realistic hardware model.

1 Introduction

Quantum computing promises speed-ups for a number of relevant computational problems. Building a scalable and reliable quantum computer is one of the challenges of modern science. As the size of quantum computers increases, the focus of interest shifts from their basic physical principles to structured design methodologies that will allow us to realise large-scale systems.

In general, quantum circuit optimisation methods are used to minimise the implementation costs like the number of gates or the number of wires [29]. Classical circuit optimisation assumes fixed gate lists even in the presence of gate errors, but classical circuits are more robust towards errors, whereas quantum information is fragile [24, Ch. 8]. Classical gate failures are usually solved either by hardening the circuit (e.g. modifying transistor sizes), or by introducing various types of information redundancies that mitigate the failures. Gate hardening is not considered realistic in quantum computing architectures, and a feasible solution requires quantum error-correcting codes (QECC) [11]. The structure and design of QECC allows encoded quantum gates to be applied directly to the encoded quantum data.
In contrast to the classical case, the most practical implementations of QECC and fault-tolerant quantum circuits are composed of gates which are non-deterministic even in the absence of errors [14]. They either work correctly or require a correction, which is only determined during the execution of the circuit. Most such correction gates do not need to be dynamically included into the executing circuit, because their effect can be classically tracked through the subsequent gates [26]. This is not true for all possible corrections occurring during the execution of a quantum circuit and some need to be actively applied to the quantum data [14]. This means that the overall circuit is dynamic, because its gate list needs to be modified during its execution based on certain measurement results. Reducing the incidence of such gates is difficult because when a fully error-corrected, fault-tolerant circuit is examined, it is exactly these measurement-based corrections that appear to give quantum computing its power [15].

In general, fault-tolerant quantum circuits are constructed from Clifford and $T$ (Section 1.1) gates, and the $T$ gate is the main source of the complications [4] for which dynamic corrections cannot be avoided.

The separation of circuit gates into Clifford and $T$ gates is generally performed at the higher level circuit design layer in order to make fault-tolerant error constructions more amenable to practical implementation. The physical mapping of these circuits to an actual error corrected architecture is then done with a specific QECC and hardware architecture in mind, preserving fault-tolerance. Fault-tolerance is understood as the set of procedures by which the cascade of quantum errors (bit and phase flips) caused by the circuit [11] is restricted allowing the underlying QECC to be effective when mapped to actual operations in a hardware model. In standard fault-tolerant constructions (those that are widely used in state-of-the-art hardware models [10,20,23,31]), the only dynamic corrections needed are when we implement logical layer corrections for $T$ gates. These correctional gates are constructed using ancillae initialised into high-fidelity states (see Section 1.5) and gate teleportation protocols [14]. Our results are quite similar to those present in Ref. [9], however this work focuses on producing a representation that is compatible with fault-tolerant error correction protocols.

The solution to having all the required corrections into the logical layer of the computation is to translate circuits into a regular representation that replaces correctional gate dynamics with the dynamics of reading and interpreting the circuit outputs. Such an approach is similar to the model of measurement based quantum computing (MBQC) [7], where a computation is solely described by the interpretation of the measurements performed on a specifically initialised quantum state. A circuit is described in this work as an ICM sequence, where the $I$ part contains qubit initialisations, the $C$ part is a sub-circuit consisting entirely of CNOT gates, and the qubits are measured in the $M$ part. This work represents a separate and distinct approach from the work of [21], where $NCV$ (reversible) circuits were mapped into Clifford and $T$ gate circuits, because the ICM representation is regular and consists entirely of ancillae, CNOTs and measurements.