The Certainty of Uncertainty: Randomness in Nanometer Design

Hongliang Chang\textsuperscript{1}, Haifeng Qian\textsuperscript{2}, and Sachin S. Sapatnekar\textsuperscript{2}

\textsuperscript{1} CSE Department
\textsuperscript{2} ECE Department
University of Minnesota, Minneapolis, MN 55455, USA

Abstract. Randomness and uncertainty are rearing their heads in surprising and contradictory ways in nanometer technologies. On the one hand, uncertainty and variability is becoming a dominant factor in the design of integrated circuits, and on the other hand, algorithms based on randomness are beginning to show great promise in solving large scale problems. This paper overviews both aspects of this issue.

1 Introduction

A historical look at integrated circuit technologies shows several inflection points that have characterized the 250nm, 180nm and 130nm nodes. The move to the sub-100nm regime is projected to bring about the most revolutionary of these changes, in terms of how it impacts the way in which design is carried out. Most notably, randomness will become a fact of life that designers will be forced to confront, and perhaps, paradoxically, the only certainty in nanometer designs will be the presence of uncertainty. Several issues related to uncertainty and randomness will be discussed in this paper.

We will begin, in Section\textsuperscript{2}, by exploring the origins of randomness in nanometer circuits, and will then discuss methods that must be used in next-generation designs to handle such variations in Section\textsuperscript{3}. This first aspect of randomness, caused by process and environmental variations, is “problematic” and requires new solutions to overcome its effects, since such variations manifest themselves as changes in the delay and power dissipation of a circuit. As a consequence, the analysis of timing will move from a purely deterministic setting to a statistical analysis, as will the analysis of leakage power, which is becoming a major component of the total power dissipation. This has already lead to intense efforts in statistical static timing analysis (SSTA) and statistical power analysis in recent years. Finding efficient solutions to these problems presents numerous new challenges, and while some first steps have been taken, many problems remain unsolved.

Amid all these problems also lies an opportunity: there is a second facet of randomness that is likely to have very positive consequences in the future, as discussed in Section\textsuperscript{4}. As the electronic design automation world becomes more educated in the use of stochastic techniques, new opportunities will arise on the
algorithmic side, as novel statistical approaches will be developed for solving design problems. This has already been set into motion: problems as diverse as capacitance extraction, power estimation, Vdd net analysis, crosstalk analysis, placement, and ESD analysis are seeing viable stochastic solution techniques. An attractive feature of the random techniques is that when used in appropriate settings, they can scale extremely well with increasing problem sizes, and for several problems, they have the potential for localized computation. This paper will overview such algorithms and raise the challenge of harnessing the power of such methods for solving the problems of tomorrow.

2 Sources of Uncertainty

Current-day integrated circuits are afflicted with a wide variety of variations that affect their performance. Essentially, under true operating conditions, the parameters chosen by the circuit designer are perturbed from their nominal values due to various types of variations. As a consequence, a single SPICE-level transistor or interconnect model (or an abstraction thereof) is seldom an adequate predictor of the exact behavior of a circuit. These sources of variation can broadly be categorized into two classes

**Process variations** result from perturbations in the fabrication process, due to which the nominal values of parameters such as the effective channel length ($L_{eff}$), the oxide thickness ($t_{ox}$), the dopant concentration ($N_a$), the transistor width ($w$), the interlayer dielectric (ILD) thickness ($t_{ILD}$), and the interconnect height and width ($h_{int}$ and $w_{int}$, respectively).

**Environmental variations** arise due to changes in the operating environment of the circuit, such as the temperature or variations in the supply voltage ($V_{dd}$ and ground) levels. There is a wide body of work on analysis techniques to determine environmental variations, both for thermal issues [8,7,20,10], and for supply net analysis [18].

Both of these types of variations can result in changes in the timing and power characteristics of a circuit.

Process variations can also be classified into the following categories:

**Inter-die variations** are the variations from die to die, and affect all the devices on same chip in the same way, e.g., they may cause all of the transistor gate lengths of devices on the same chip to be larger or all of them to be smaller.

**Intra-die variations** correspond to variability within a single chip, and may affect different devices differently on the same chip, e.g., they may result in some devices having smaller oxide thicknesses than the nominal, while others may have larger oxide thicknesses.

Inter-die variations have been a longstanding design issue, and for several decades, designers have striven to make their circuits robust under the unpredictability of such variations. This has typically been achieved by simulating the