12 Phase Locked Loops and Synthesisers

In the preceding chapter we have observed that the frequency stability of oscillators is significantly deteriorated by noise. Moreover, we have to consider the impact of process variations, temperature changes and aging. These effects make it impossible to reproduce a certain oscillation frequency at given varactor voltage. To meet the challenging requirements in synthesisers, tracking filters, clock recovery circuits and PLL (Phase Locked Loop) techniques are commonly applied. Referring to Sect. 11.4, phase noise and jitter appearing in the frequency and time domain, respectively, are useful measures for the signal purity. PLLs can be realised in analogue, digital or mixed analogue/digital form. In this chapter, we focus on analogue PLLs, which have lower complexity than their digital counterparts.

PLL based systems are nonlinear. Due to the interdependencies of the inherent components analytical and numerical analyses are complex. As for other circuits, we can make life much easier by linearisation of the dynamic operation around a static operation point exhibiting average characteristics. Usually, this simplification provides good accuracy as long as the elongations around the static operation point are small. These simplified analyses are sufficient to understand the fundamental relations. Further optimisations are usually made on basis of CAD tools and large signal simulations.

For detailed information about PLLs, the reader is referred to the specific literature [Bes93, Raz96, Rat01].

12.1 Phase Locked Loop Basics

A PLL synchronises the output by means of a reference input. Feedback from the output to the input is employed for this task. The parameter to be locked in communication systems is the frequency. In the locked case, the input and output frequencies $\omega_\text{in}$ and $\omega_\text{out}$ are equal. The phase is the integral of the frequency implying that in locked state the phase difference $\Delta \varphi(t)$ between the input and output phase $\varphi_\text{in}(t)$ and $\varphi_\text{out}(t)$ must be constant demanding for $\frac{d\varphi_\text{out}}{dt} - \frac{d\varphi_\text{in}}{dt} = 0$ and subsequently $\omega_\text{out} = \omega_\text{in}$. The latter property will serve as an important control goal.

Life is a face locked loop.
Unknown
We can conclude that in the locked state, the input and output signals are synchronised in frequency and phase. An unlocked loop yields $\omega_{\text{in}} \neq \omega_{\text{out}}$ and exhibits a $\Delta \phi$ varying with time. Referring to the block diagram in Fig. 12.1, the PLL mainly consists of a VCO (Voltage controlled Oscillator), a PD (Phase Detector) and a LP (Lowpass) filter. These components will be treated in the following sections. There are three key parameters that are of particular importance in practical systems:

- Capture range: input/reference frequency range for which the loop can achieve lock.
- Lock range: input/reference frequency range over which the loop will remain locked – usually larger than capture range.
- Settling time: required time for the loop to lock onto a new frequency.

![Fig. 12.1. Block diagram of basic PLL in time domain](image)

### 12.1.1 Phase Detector

The main task of the PD is the detection of the phase difference between two signals. Hence, the PD may be described as an error amplifier. In the PLL, the phase difference or phase error is given by $\Delta \phi(t) = \varphi_{\text{out}}(t) - \varphi_{\text{in}}(t)$. Dependent on this phase difference, an output voltage $v_{PD}(t)$ is generated in the phase detector. For analysis and further processing it is convenient if this relation is linear. Referring to Fig. 12.2a, we may write

$$v_{PD}(t) = K_{PD} \cdot \Delta \phi(t) \quad (12.1)$$

where the slope $K_{PD}$ has a unit of V/rad. Let’s review these idealised characteristics with real word circuits. Mixer based phase detectors are frequently employed as phase detectors. One example is the Gilbert cell mixer treated in Sect. 10.3.3. The circuit acts as signal multiplier. Corresponding theoretical background can also be found in Sect. 4.4.3. After adequate filtering, multiplication of the input signals $v_{\text{in}}(t) = V_{\text{in}} \cos(\omega_1 t)$ and $v_{\text{out}}(t) = V_{\text{out}} \cos(\omega_2 t + \Delta \phi)$ yields the following dependency:

$$v_{PD}(t) = c \cdot \cos \left[ \left( \omega_2 - \omega_1 \right) t - \Delta \phi \right] \quad (12.2)$$

with $c = V_{\text{in}} \cdot V_{\text{out}}$ as the device specific conversion coefficient. Assuming $\omega_{\text{in}} = \omega_{\text{out}}$ yields

$$v_{PD}(t) = c \cdot \cos \Delta \phi \quad . \quad (12.3)$$