High $\kappa$ Gate Dielectrics for Compound Semiconductors

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Summary. The ability of controlling the growth and interfaces of ultra-thin dielectric films on compound semiconductors by ultrahigh vacuum physical vapor deposition has led to comprehensive studies of gate stacks employing high $\kappa$ gate oxide $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$ and rare earth oxide $\text{Gd}_2\text{O}_3$. These oxides as gate dielectrics on GaAs have been shown to possess a low interfacial density of states, thus solving a problem which has puzzled researches for almost four decades. The electrical, thermal, chemical, and structural properties of these novel oxides and their interfaces with GaAs are reviewed. Particularly the achievement of low interfacial density of states ($D_{it}$) and thermodynamic stability upon high temperature annealing is discussed. The interfacial oxide layers on GaAs were found to be a single crystal of pure $\text{Gd}_2\text{O}_3$. The ultra-thin $\text{Gd}_2\text{O}_3$ on GaAs has given a very low leakage current and low $D_{it}$, a first time achieved by a single crystal oxide. Various GaAs metal-oxide-semiconductor field-effect-transistors (MOSFETs) and their device performance are reviewed. The mechanism of Fermi-level unpinning in ALD-$\text{Al}_2\text{O}_3$ on InGaAs was studied and understood. The epitaxy and the interfaces of $\text{Gd}_2\text{O}_3$ on GaN were characterized, and show strong tendency to conform to the underlying substrate, thus providing insight into the fundamental mechanism for low interfacial state density and effective passivation. These gate stacks of abrupt interfaces and controlled microstructures were employed as a model system to elucidate critical issues of materials integration in the CMOS process.

10.1 Introduction

The Si technology is entering the age of nano-meters, with the gate length of 90 nm in production and devices of 50 nm or smaller in research and development. Up to now, the level of perfection in the well known Si–SiO$_2$ interface enables the design and large-scale applications of complementary metal-oxide-semiconductor (CMOS) transistors and integrated circuits. The rapid shrinkage of transistor feature size in Si CMOS scaling has forced the channel length to decrease to be around 15 nm by year 2010, and the SiO$_2$ gate oxide thickness is correspondingly reduced to be close to the quantum tunneling limit of
1.0 nm. Beyond this point leakage current due to tunneling, $\sim 1-10$ A cm$^{-2}$, becomes the dominant leakage mechanism in device designs. There is another ultimate physical limit below which SiO$_2$ no longer maintains its bulk electronic structure [1], and this appears to be about 0.7 nm.

The current trend of Si CMOS scaling thus calls for replacing SiO$_2$ with high $\kappa$ dielectrics in gate related applications [2]. Over the last five years of intense research on high $\kappa$ gate dielectrics, a number of binary oxides and silicates in amorphous form have emerged [2–7], and shown impressive dielectric properties with an equivalent oxide thickness (EOT), defined as $t_{eq} (\frac{\kappa_{SiO_2}}{\kappa_{oxide}})$, as thin as 1.0 nm. To achieve performance comparable to SiO$_2$, the new high $\kappa$ dielectric materials must satisfy very stringent requirements for the fundamental properties such as dielectric constant, band gap, conduction band offset, leakage, mobility, and good thermodynamic stability in contact with Si up to 1,000°C. It is equally critical to address device processing and integration issues such as morphology, interfacial structure and reactions, gate and process compatibility, and reliability.

Among these challenges, the mobility degradation due to the high $\kappa$ gate dielectrics is the most difficult issue. High Coulomb scattering rate from charge trapping may lead to poor channel mobility. In order to overcome the degraded channel mobility encountered in the high $\kappa$ gate stacks on Si, channel materials with higher carrier mobility such as strained Si, Si–Ge alloys, and Ge are being studied, and the strained Si is now being used in the production.

It is known that electrons move much faster in GaAs (and other III–V compound semiconductors) than those in Si, and Ge, an important aspect for building high-speed devices. Furthermore, semi-insulating substrates, not available in Si and Ge, will reduce cross talks between high-speed signal lines in dense circuits. A mature compound semiconductor technology (particularly III–V MOS devices) with electron mobilities at least 10 times higher than that in Si and with dielectrics having $\kappa$ several times higher that that of SiO$_2$ would certainly enable the electronic industry to continue pushing its new frontiers for a few more decades. Furthermore, bandgap engineering and direct bandgaps, not available in Si-based material systems, provide novel designs and make highly performed integrated optoelectronic circuits (combining MOS and photonic devices) a reality.

For microwave and digital applications, III–V MOSFET’s promise the advantage of low power consumption and circuit simplicity, comparing with the present devices based on MESFET or HEMT technologies, which have encountered inevitable current leakage through the Schottky metal gates. In the area of high power devices, the high band-gaps in the compound semiconductors (e.g., 1.42 eV in GaAs and 3.2 eV in GaN, comparing with 1.1 eV in Si) have provided intrinsic advantages such as larger bulk breakdown fields over the present Si technology (1.1 eV in Si). Their intrinsic high bandgap and breakdown fields make them natural candidates for high power electronic devices operated at high temperatures. Particularly, GaN-based MOSFET or MOHEMT are the choice of devices for the very high power applications.