Design of the Tile-Based Embedded Multimedia Processor –TEMP–

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Abstract. An advanced multimedia processing unit is needed for the DVD player, the music player, and the video game machine, etc., we propose a sub-processor for advanced multimedia processing for built-in usage. We achieve the necessary arithmetic capacity equal with the processing, only for the multimedia by proposing multimedia processing is done by extended instruction. The tile processor is adopted as architecture of the processor. The tile processor can reduce the wiring delay that happens because of tile positioning, and is suitable for the miniaturization required for built-in processors. Moreover, the high parallel processing ability of the tile architecture is the best for media operations involving same operation and repetitions of data volume. With the aim of time efficiency, SIMD style operation was installed. However with device miniaturization a high level of integrations necessary

Keywords: Embedded System, Tile-Based Processor.

1 Introduction

The rapid evolution of multimedia due to the spread of the Internet in the latter half of the 20th century has created demand for devices such as cellular phones and DVD players, with high-speed voice image data processing. For this, the ability to execute the image data processing and the voice processing, etc. in real time is necessary. As a result, the multimedia processor appeared in general-purpose CPUs which depended on a multimedia extension instruction with special MMX instructions. Given the nature of the miniaturization (embedding multimedia capable processors etc) it follows that a high level of integration is necessary. It fallows too that RSP and reliability are also demanded. So, we propose tile architecture and SIMD type multimedia extension instruction for the multimedia processing which is appropriate for built-in processors using reduced time interval.

The wiring delay often found in processors with a high level of integration built in is significantly reduced with tile architecture. This design reduces the wiring delay between tiles by limiting communication proximity only to/and between tiles in close physical.

T. Enokido, L. Barolli, and M. Takizawa (Eds.): NBiS 2007, LNCS 4658, pp. 505–512, 2007.

The SIMD (Single Instruction Multiple Data) instruction is an instruction, via which two or more pieces of data can be processed by one instruction. As SIMD allows high speed operations, such as simultaneous processing and repetition processing, image processing and filtering processing for voice processing is possible. Moreover, it becomes easy to change and debug the algorithm because it is program based rather than hard-wired. It follows then that Rapid System Prottyping (RSP) can be assured. In this paper, the enhanced instruction set for multimedia, in accordance with INTEL MMX, is defined and implemented on tile architecture.

2 Related Works

2.1 TRIPS

The tile processor named TRIPS presently under research at Texas University utilizes a concept of data flow architecture [1]. TRIPS consists of 16 processing elements in 4×4 arrays, which consist of integer units, floating point arithmetic units, input ports, output ports, operand buffers, and routers. The 16 (4 x 4) processing arrays are the main core, and the instruction cache, the data cache, and the registers are located in the immediate surroundings of the core. Each tile communicates with adjacent tiles. Each tile executes the instruction as soon as data arrives. This part looks like the architecture of the data flow machine. In the case of instruction fetch, delay occurs. To eliminate this delay, two or more instructions are fetched at the same time.

Figure 1 shows the block diagram of 4×4 TRIPS processors.

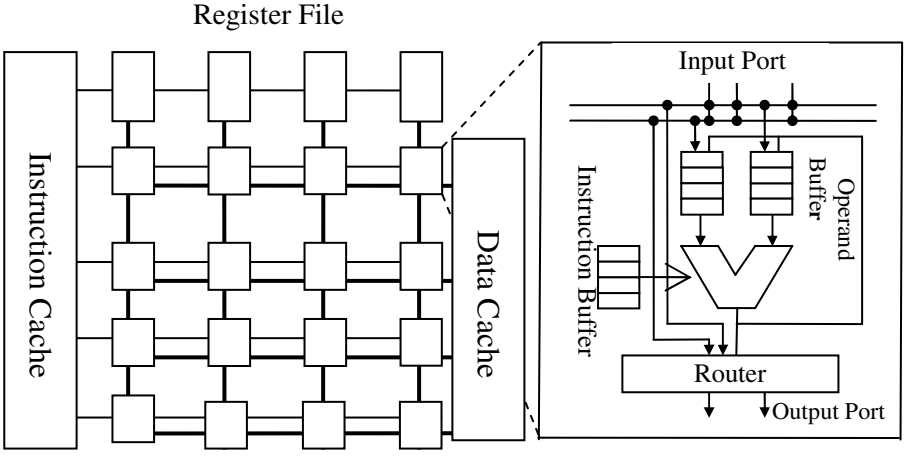

Fig. 1. Block diagram of 4×4 TRIPS processor

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