# A Bumpless Switching Scheme for Dynamic Reconfiguration

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**Abstract.** The bumpless switching is a concept from cybernetics. It refers to the smooth switching condition when a new system replaces the old one in operation. We implemented the dynamic reconfiguration of SoC based on delta MPU architecture to reach a bumpless switching. The dynamic reconfiguration of SoC with bumpless switching depends on a co-design of some bumpless switching algorithm and a SoC hardware with delta core structure. Since bumpless is a desired condition in system switching, the scheme is significant for the dynamic reconfiguration of SoC.

**Keywords:** bumpless switching, SoC, dynamic reconfiguration.

## 1 Bumpless Switching and Dynamic Reconfiguration of SoC

The bumpless switching is a concept in cybernetics [1]. It refers to a smooth condition of a new system replacing the old one in operation. A bumpless switching means the switching is smooth. The concept is introduced here.

The transfer matrices of a system in the state space are as follows [2].

$$\dot{x}(t) = Ax(t) + Bu(t)$$

$$y(t) = Cx(t) + Du(t)$$

Where, y(t) is the output; u(t) is the input; and x(t) is the state variable; A, B,C and D are gain matrices.

$$A = \begin{bmatrix} A_{11} & \dots & A_{n1} \\ \dots & \dots & \dots \\ A_{1n} & \dots & A_{nn} \end{bmatrix}$$

$$B = \begin{bmatrix} B_{11} & \dots & B_{n1} \\ \dots & \dots & \dots \\ B_{1n} & \dots & B_{nn} \end{bmatrix}$$

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The matrices C and D are similar to A and B. If A, B switch value and C, D remain fixed (i.e. C and D are constant matrices), the system is said to be bumpless.

Actually, we can call a switching system bumpless if its output *y(t)* remains a continuous function of time, even during a change of transfer matrices, provided that its input *u(t)* is continuous. Otherwise, the system switching is called bumpy.

For most SoC, System on a Chip, applications, the function of the state space is zero order. And the C and D are fixed constant matrices. Assuming a SoC system with zero order, for example its state space can be described as

$$y(t) = Cx(t) + Du(t)$$

$$C = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad D = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}.$$

When C and D are constant matrices, the system switching is bumpless. The switching result for a DRSoC, Dynamic Reconfiguration SoC, depends on the input parameters of SoC and some adjustment algorithm [3]. Normally a SoC in operation is a steady and controllable system with zero order description of state space [4]. Therefore, as a controlled system, SoC is simpler, and its algorithm of bumpless switching is easier fetched.

## 2 A Scheme of Bumpless Switching for SoC with Delta Core

The dynamic reconfiguration of SoC with bumpless switching depends on a co-design [5], the combination of some bumpless switching algorithm and a SoC hardware with delta core structure.

There are three MPUs embedded in the SoC with delta core. They are monitor MPU, operating MPU and backup MPU respectively. The structure of operating and backup MPU is similar. They may be considered as twin cores.

The algorithm of bumpless switching is embedded monitor MPU. In most cases, the backup MPU with similar algorithm to operating MPU, the monitor MPU detects the output status of backup MPU [6]. When the running state of backup MPU is statically closed to operating MPU. The monitor MPU realizes some instructions to transfer the backup MPU as a new operating MPU. The original operating MPU would become a backup MPU. When the inputs/outputs of the MPU cores are consistent and the timing control is available, the switching procedure may be bumpless. If the original operating MPU is replaced by the new operating MPU, the SoC is reconfigured or repaired.

In order to take a solution for SoC dynamic reconfiguration with bumpless switching, so far, we have designed and simulated some switching circuit based on FPGA with VHDL. A basic output cell of the circuit is shown as Fig.1. The MPU1 and MPU2 in Fig.1 are two cores in the SoC. One is operating core. Another is backup core. The out1 in Fig.1 means output1 of a MPU. May there be n outputs for a MPU. They are out1 to outn.