A Novel Routing Architecture for Field-Programmable Gate-Arrays

Alexander Danilin¹, Martijn Bennebroek², and Sergei Sawitzki¹

¹ NXP Semiconductors
Corporate Innovation and Technology, Research Division
High Tech Campus 32
5656AE Eindhoven, The Netherlands
{Alexander.Danilin,Sergei.Sawitzki}@nxp.com

² Philips Research Europe
High Tech Campus 5
5656AE Eindhoven, The Netherlands
martijn.bennebroek@philips.com

Abstract. A novel routing fabric is introduced that offers high flexibility at significantly lower silicon cost compared to routing fabrics currently incorporated in Field Programmable Gate Array (FPGA) devices, IP cores, and IP-core wrappers. This fabric is entirely constructed from multiplexers and unidirectional point-to-point connections, controlled by configuration bits. Key in optimizing its efficiency is to derive an appropriate connectivity pattern between logic blocks. Although this problem is complex in general, three guidelines have been identified to define suitable patterns. For a fabric connecting 4-input Look-Up-Tables, area savings of 60% are demonstrated when routing applications from the MCNC benchmark set. The use of multiplexer-based routing is not limited to these basic logic blocks only, so the potential of its usage for more complex logic blocks is illustrated as well. Benefits in timing closure, performance, and power are briefly discussed.

1 Introduction and Previous Work

Reconfigurable logic offers great flexibility with respect to standard-cell logic though at significant area, power, and delay penalties. The main culprit is the configurable routing fabric that consumes most of the silicon area and, even worse, is often not utilized efficiently when mapping applications. Therefore, academic and industrial effort has been and still is devoted to further improve routing fabrics traditionally in stand-alone devices but, more recently, also in embedded IP cores and IP core wrappers. Most commercial Field Programmable Gate Array (FPGA) devices, including the recent families of Xilinx and Altera, use a Manhattan routing fabric [1] schematically depicted in Fig. 1. Such routing fabrics are also known as mesh-based [1] or island-style [2]. Here, logic blocks are connected by connection boxes to adjacent horizontal and vertical routing channels.
The wire segments in a channel can be of various lengths, from short (spanning a single or few logic blocks) to medium (four to sixteen logic blocks) and long (spanning half a die or even a full die). Switch boxes are located at the channel intersections to enable wire segments to be connected in any direction, horizontally or vertically, and thereby to route signals between any logic and/or IO blocks in the two-dimensional array. The main challenge in designing (Manhattan) routing fabrics is to achieve routability for a wide variety of applications with a minimum of routing resources such that the utilization density of logic blocks is maximized (whereby signal speeds and power consumption are still acceptable). In reality, Manhattan routing fabrics are designed based on best practices and incorporate a wealth of routing resources that dominate the FPGA area. For example, in [1] it is reported that 84% to 92% of the FPGA area is consumed by the routing fabric. The FPGA architectures studied in [1] contain logic blocks with clusters of six 4-LUTs. For FPGA architectures containing simpler logic blocks, the area consumption may become even more extreme and (for one of the FPGA architectures discussed later in this paper with only a single 4-LUT logic block) even amount to 95%. Manhattan routing fabrics themselves