Chapter 13
Impedance Spectroscopy as a Powerful Tool for Better Understanding and Controlling the Pore Growth Mechanism in Semiconductors


Abstract This work shows new results toward a better understanding of macropore growth in semiconductors by using in situ FFT impedance spectroscopy. A new interpretation of the voltage impedance is proposed. In particular, the pore quality could be quantified for the first time in situ, especially by extracting the valence of the electrochemical process. The study paves the way toward an automatized etching system where the pore etching parameters are adjusted in situ during the pore etching process.

13.1 Introduction

The electrochemical pore formation in Si is a topic [1] with many potential applications, and much progress was made toward the development of production technologies [2] and many product prototypes were advanced (see [3] and references therein). Despite all of this work, no product based on porous Si can be found on the market at present. Among the main reasons for this is the still-not-fully-understood mechanism of pore formation, or more generally, the many open questions in the field of electrochemistry of semiconductors. As an example, many envisioned applications demand precise control of the pore quality (e.g. diameter variations, pore wall roughness) and the present understanding of pore formation mechanisms, although rather advanced in some respects, does not ensure full control of the etching process as would be needed.

In this work, we show how impedance spectroscopy can be used for the purpose of controlling the macropore growth in n-type Si. In particular, it is shown how one can extract the dissolution valence at the pore tips from the measured impedance. This number is used as a quantification of the pore quality. Determining this number in situ can pave the way toward the implementation of an automatized etching system.
13.2 Experimental

n-Type Si wafers with low doping levels corresponding to a resistivity of 5 Ω cm are used for etching macropores. The substrate orientation is (100) with an n⁺ layer on the backside of the wafer for a good ohmic contact to the sample. The etching is done using backside illumination (BSI) [4]. The samples were prestructured by standard photolithography before etching; the nucleation pattern was a hexagonal lattice with a lattice constant of $a = 4.2 \, \mu\text{m}$. The electrolyte consisted of 5 wt.% HF in an aqueous electrolyte. The temperature of the electrolyte was fixed at 20°C. The FFT impedance spectrometer embedded within the etching system provided by the ET&TE GmbH, Germany was used to extract information concerning pore growth during the etching process.

13.3 Results and Discussion

For voltage impedance, a small perturbation signal is applied to the anodization voltage and the response in the etching current is measured. Figure 13.1a shows the $I-V$ curve of n-type Si in contact with HF under BSI. One can easily see that a change in the voltage causes a variation in the current. Since during the macropore etching the etching voltage must be in the saturation regime of the $I-V$ curve [2], the linearity condition is fully fulfilled. However, another problem can be seen, i.e., being in the saturation regime, any perturbation in the voltage generates a minute variation of the current. In order to separate the measured signal from noise, strong requirements are imposed to the measuring hardware as well as to the data processing software.

Figure 13.1b shows a typical Nyquist plot of the measured impedance. The squares indicate the measured data. The data are fitted using the following model:

![Graph](image-url)