Chapter 7
FSM Synthesis with Object Code Transformation

Abstract. The chapter is devoted to original optimization methods oriented on decrease of the number of outputs for FSM block generating input memory functions. These methods are based on the object code transformation. The FSM objects are either states or collections of microoperations. Sometimes, some additional identifiers are needed for one-to-one representation of different objects. Such optimization methods are discussed for both Mealy and Moore finite state machines. At last, the multilevel models of FSM with object code transformation, logical condition replacement and encoding of collections of microoperations are discussed. This chapter is written together with employee of "Nokia-Siemens Network" Alexander Barkalov (Ukraine).

7.1 Principle of Object Code Transformation

As it was mentioned before, the hardware reduction for FSM logic circuit is connected with the structural decomposition, which in turn is connected with increase for the number of levels in the FSM model. To optimize the hardware amount in block BY, it is necessary to generate some additional variables for encoding of microoperations (or collections of microoperations). The methods discussed in this Chapter are taken from [2–6]. These methods are based on one-to-one match among collections of microoperations and states. Let us name as objects of FSM its internal states \( a_m \in A \) and collections of microoperations \( Y_t \subseteq Y \). Let us point out that states and collections of microoperations are heterogeneous objects respectively each other, whereas different states, for example, are homogenous respectively each other. The optimization methods discussed in this Chapter are based on identification of one-to-one match among heterogeneous objects. If this match is found, then the block BP generates only codes for one object (which is a primary object), while a special code transformer generates the codes of another object (which is a secondary object).

Let us find a one-to-one match \( A \rightarrow Y \) among the states as primary objects and the microoperations as secondary objects. In this case, the block BP generates input
memory functions $T_r \in T = \{T_1, \ldots, T_R\}$ to encode the states, whereas a special state code transformer block TSM generates variables $z_r \in Z$ used for encoding of collections of microoperations. The structural diagram of Mealy FSM based on this principle is shown in Fig. 7.1. Let the symbol PC_{AY} stand for this model if collections of microoperations are encoded, whereas the symbol PC_{AD} stands for encoding of the classes of compatible microoperations. Let us name such models as FSM1.

Let us find a one-to-one match $Y \rightarrow A$ among the microoperations as primary objects and the states as secondary objects. In this case, the block BP generates variables $z_r \in Z$, whereas a special microoperation code transformer block TMS generates input memory functions $T_r \in T$. This approach results in the models of FSM2, denoted as PC_{Y\ Y} (if collections of microoperations are encoded) or as PC_{Y\ D} (if classes of compatible microoperations are encoded). Their structural diagram is shown in Fig. 7.2.

These models correspond to cases when an FSM has the same numbers of states and collections of microoperations. If this condition is violated, then some additional identifiers should be used belonging to a set of identifiers $V$. In common case, the block BP generates variables $T$ and $V$ (Fig. 7.3) or variables $Z$ and $V$ (Fig. 7.4). All these variables are the outputs of the register RG.

Thus, in common case the number of bits in the register RG for Mealy FSM with object code transformation exceeds this number for equivalent PY or PD Mealy FSM. Obviously, the proposed approach can be applied iff the total hardware amount for blocks BP and TSM (TMS) is less, than the hardware amount for block BP of PY (PD) Mealy FSM. The same approach can be applied for Moore FSM. Let us point out that only application of the proposed approaches allows the economical implementation of PD Moore FSM.