A Quick Method for Mapping Cores Onto 2D-Mesh Based Networks on Chip*

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Abstract. With the development of NoC, it becomes an urgent task to efficiently map a complex application onto a specified NoC platform. In the paper, an approach which is called constraint-cluster based simulated annealing (CCSA) is proposed to tackle the mapping problem in 2D-mesh NoC in order to optimize communication energy and execution time. Different from other methods, the relationship among cores that are partitioned into several clusters is considered in our method and according to the relationship constraints are set. Experimental results show that the proposed approach gets shorter execution time with lower energy consumption compared with others algorithms. In VOPD application (4x4), the reduction of execution time is about 75.64% combing the normal simulated annealing. In greater application (8x8 vodx4) the CCSA can save 68.89% . The energy consumption is the lowest among all the compared algorithms.

Keywords: network on a chip (NoC) Application mapping Simulated Annealing.

1 Introduction

With the advance of Semiconductor, the number of transistors available will be more than 4 billion at more than 10Ghzspeed[1].This allows that more than dozens of IP-blocks can be integrated in a single chip. Different from dedicated wires and shared-medium busses, the network on a chip (NoC) provides a high performance chip-level communication with regularity and modularity.

In literature[2] formulated the 32bit’s ALU power consumption is about 0.3 pj,while translate 32 bits over 10mm need 17pj, the consumption of translation is more the 50 times than Alu. So how to decrease the energy consumption of a single chip is a challenging job in NoC platform. In the design flow for NoC architecture , the step of Mapping which determines which nodes host which cores is very important These choices have significant impacts on energy, area and performance metrics of the system[3],[4].

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The core-to-node mapping problem is a NP-Hard optimization problem [3]. For the node number of N, the result of mapping will be N! . The computation and search space are very huge. For example, mapping 16 cores onto 16 nodes has a search space of 16! , that is about $2.1 \times 10^{13}$. The count of computation of each map is about 435 Flop. Thus the computation is about 1016. Suppose the computer is Intel 3.0 GHZ four cores, it will cost about 120 hours to fulfill the searching. So some efficient analytical model which can be used to find nearly optimal solutions in reasonable time must be presented.

In this paper, we present a rapid algorithm named Constraint-cluster based Simulated Annealing Approach (CCSA) to minimize the power consumed and overall runtime. The node can be partitioned into some cluster by calculating the communication difference between nodes, and according to the partition some searching restriction can be set. A cluster partition can make the problem more easy. Just as what has discussed above, for 16 cores/nodes, if they can be portioned into some clusters, the 16! problem would be a $N! \times C_1! \times C_2! \times \ldots \times C_N!$ problem, which is smaller than 16! to search. In the course of searching, the searching space is limited by the cluster restriction. By the partition and constraint the algorithm can resolve the mapping quickly without reducing the quality of solution. This paper chooses a two dimensional mesh interconnection which is very simple from a layout perspective and the local interconnections between resources and switches are independent of the size of the network. Moreover, routing in a two dimensional mesh is very easy resulting in potentially small switches, high bandwidth, short clock cycle, and overall scalability.

The rest of the paper is organized as follows. We define the mapping problem and give an overview of our Constraint-cluster based Simulated Annealing Approach (CCSA). Then the CCSA in details is described. The experimental results are reported in the last.

2 Related Works

Now NoC mapping problem has become a broad topic of research and development. In [3], Hu and Marculescu presented a static mapping a branch-and-bound algorithm. The main goal of the approach is to reduce the overall power consumption by decreasing the consumed energy on communication. Literature [5] presents a two-step genetic algorithm to map an application, described on a mesh-based NoC architecture with the objective of minimal execution time. Zhou et al. apply a queue model to calculate the latency of net. In paper [7] a communication model is accept to calculate the latency of communication. In [6] another communication model is proposed to calculate the latency. In [12] PMAP, a two-phase mapping algorithm for placing the clusters onto processors is presented. The results of PMAP algorithm are shown to have low communication costs. In [11] Murali and De Micheli proposed a rapid algorithm NMAP that maps the cores onto mesh NoC architecture under bandwidth constraints. In general those algorithm dose not consider the characteristics of nodes in the no-heuristic search, so the search methods must balance the run time and the quality of result (such as branch-and-bound or back-tracking). A heuristic method may