Crystal Defects and Electrical Properties in Ion-Implanted Silicon

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Abstract

Investigations have been made on crystal damages in silicon produced by 100 and 150 keV B⁺, P⁺, and Ne⁺ ion implantations. Their effects on electrical properties of the implanted layers have also been studied as a function of implantation and subsequent annealing conditions.

Secondary defects in ion-implanted silicon have recently been observed by transmission electron microscope [1-9]. However, on the correlations between such defects and electrical properties of the ion-implanted layers, enough informations have not been reported except the correlations between sheet resistivity and electron microscope observations in B⁺ implanted and annealed silicon by Bicknell and Allen [5].

We have compared the annealing characteristics of secondary defects with such electrical properties as carrier concentrations and mobilities, and the diffusion length of minority carriers. Furthermore, on the basis of the fact that there were clear differences in annealing characteristics of carrier concentrations, when implantations were carried out in different temperatures, the changes in annealing behavior of secondary defects were studied between room and hot implanted samples with P⁺ ions. The depth distributions of defects were also compared with carrier concentration profiles.

B⁺, P⁺, and Ne⁺ ions with doses between \(1 \cdot 10^{14}\) and \(1 \cdot 10^{16}/\text{cm}^2\) were implanted at 100 and 150 keV into (111) oriented, 10 Ω-cm p- and n-type silicon wafers. Implantations were made between room temperature and 750°C. Before the measurements, implanted wafers were isochronally annealed for temperatures up to 1200°C in a nitrogen atmosphere.

Defects in implanted layers were observed by transmission electron microscope of 100 keV and 1000 keV with the specimen tilting and rotating mechanism.
Samples for electron microscopy were thinned from the side opposite the implanted surfaces by the standard chemical etching method.

To remove the implanted layers in 500 Å steps, the anodic oxidation and stripping techniques were employed. To determine the distributions of carrier concentrations and crystal damages at various depths within implanted layers, sheet resistivity and Hall effect measurements by van der Pauw's method and electron microscope observations were made on the new surfaces thus formed. The diffusion length of minority carriers in implanted layers was measured by a scanning electron microscope, in which an electron beam was bombarded into boron diffused p⁺-n junction diodes which were implanted by Ne⁺ ions. Short circuit junction current during electron bombardment was measured as a function of minority carrier diffusion length.

Effect of Annealing Temperatures

Table 1 shows the summary of annealing effects on defects and electrical properties of silicon crystals implanted with B⁺, P⁺ and Ne⁺ ions at room temperature. Primary defects disappeared by annealing at temperatures below 600 °C. Above 600 °C secondary defects such as dislocation loops, stacking faults, precipitates and dislocation networks began to be detected by electron microscope.

Table 1. Annealing characteristics of B⁺, P⁺ and Ne⁺ implantations into silicon.

The recovery of carrier concentrations depended upon whether amorphous layers were formed during implantation or not, and carrier concentrations were completely recovered by annealing near 1000 °C. However, the lifetime of minority carriers in the implanted layers was considerably shorter than that of the carriers in the diffused layers even after 1000 °C annealing treatment. The change in secondary defects which was observed in the same samples as minority carrier lifetime samples was strongly dependent upon annealing temperatures. In high temperature,