Bus Arbitration Concepts For
The Fifth Generation Advance

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ABSTRACT
Through the use of massive parallelism, Intelligent Memory offers many solutions to software problems. However bus interaction and contention remains a major problem. This paper addresses these problems and highlights possible solutions.
1.0 Background.

The proposed advances in 5th Generation Computing Systems aim to provide an Intelligent Image to the system user. While such images are software based, written in languages such as Prolog and LISP, much of the proposed hardware architecture has lacked innovation and vision. This paper addresses these two important points by providing an insight into modern Bus architectures for multiprocessor systems. In order that unique system architectures may evolve; a hierarchical bus arbitration structure is proposed.

1.1 Introduction

A cloud of uncertainty hangs over the physical image that 5th generation computing systems will adopt. Therefore in this paper, the architecture of a computer system is presented as a functional module structure, together with its operation. This presentation is oriented towards V.L.S.I. realisation of the various modules that will eventually make up a typical 5th Generation computer system. These modules will become sub-system components that will be integrated into an overall system architecture supporting hardware and software extensibility. These separate, but coupled modules, are interconnected by a common bus structure and supervised by the Bus Arbitration Mechanism.