4 Analog Multiplexing DAC (AMUX-DAC)

In the previous chapter, the TI-DAC concept was introduced, which enhances the DAC sampling rate. In this chapter, the AMUX-DAC concept is addressed, which enhances both the sampling rate and the analog bandwidth.

A short introductory literature overview is followed by the description of the AMUX-DAC concept. Then, an analytical system model for $N$ DACs is derived, which has not been available in the literature up to now. Based on this, a MIMO system model is derived for the case of two DACs and extended towards $N$ DACs. Signal processing aspects are discussed next, covering both calibration requirements and DSP algorithms including algorithmic complexity estimations. A novel MIMO algorithm is derived from the MIMO system model, which mitigates the impairments also for signal paths with unequal frequency responses.

Thereafter, a general impairment model for the AMUX-DAC is introduced. Based on this, a behavioral 2:1 AMUX model for system-level simulation is developed [43]. With this model, the impact of various parameters on the combined output signal is investigated both for the AMUX by itself and for the AMUX-DAC. Furthermore, the performance of the novel MIMO equalizer is compared to a single-input single-output (SISO) equalizer.

The performance of an AMUX IC with the highest bandwidth reported at that time [42] is evaluated by an on-chip S-parameter measurement and an on-chip time-domain measurement [42]. Finally, a scaling model is introduced, limitations and challenges of the AMUX-DAC concept are described and the chapter is summarized.

4.1 Introduction

For the AMUX-DAC concept, a high-speed AMUX switches between multiple DAC output signals to aggregate these signals. Due to the nonlinear switching operation, the combined output signal has both an increased sampling rate and a higher bandwidth compared to a single DAC while assuming that the AMUX bandwidth is greater than the DAC bandwidth [47, 172].

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The concept was introduced in 2011 by Ferenci [174], who demonstrated an InP AMUX operating up to 50 GHz. A 2:1 AMUX integrated with two DACs on a single IC in 28 nm CMOS was presented with 9 bit and 11 GS/s in 2015 [219].

Recently, an 80 GBd signal with 40 GHz bandwidth was generated by multiplexing the outputs of two CMOS DACs. The DACs and the AMUX have analog 3 dB bandwidths of ~20 GHz and > 50 GHz, respectively [172, 217]. Two sub-signals with a signal bandwidth of 20 GHz each were combined with the AMUX operating at a clock frequency of 43.3 GHz. Later, the same authors showed the generation of a 300 Gb/s DMT signal with a halved clock frequency of 37.5 GHz and digital pre-processing in [173]. These authors later presented an AMUX module with an analog bandwidth of 63 GHz operating up to 128 GS/s [218] and an 2:1 AMUX IC with an analog bandwidth > 110 GHz [175].

In [42], a SiGe AMUX with an analog bandwidth > 67 GHz is presented, which was the highest bandwidth reported at that time. This AMUX is later used both as a basis for the behavioral model in Sec. 4.6 and for the measurement sections in Sec. 4.10.

By realizing the complex DAC architecture in energy-efficient CMOS technology and the analog front-end in high-bandwidth bipolar technology (SiGe, InP, etc.), all of high bandwidth, high sampling rate, and high resolution could be achieved.

As outlined both above and in Sec. 2.7.3, only a limited number of research results for high-speed switching have been published so far. Consequently, the high-speed operation of these devices requires additional investigation.

### 4.2 Concept

In Fig. 4.1, the AMUX-DAC concept is visualized. In Fig. 4.1(a), a conceptual block diagram is depicted for the case of two DACs: the outputs of the DACs are combined with the 2:1 AMUX to generate the AMUX output signal \( y(t) \). Both DACs are operated at the same sampling rate and are clocked with an 180° phase shift. The DAC input signals are denoted as \( x_1(k) \) and \( x_2(k) \). The AMUX operates in a half-clock configuration, i.e., the input signals are switched through in an alternating fashion by the positive and the negative half of the alternating clock signal. A full-rate DAC clock signal is assumed for this exemplary configuration.

In Fig. 4.1(b), the idealized operation of the AMUX-DAC is depicted in the time domain for NRZ signals. The AMUX is transparent for the DAC output signals in the center of each sample, which is denoted with a drawn-through line. In this switching period, the other input signal is isolated from the output. The isolated