5. Analysis and Compensation of the Bitline Multiplexer

5.1 Introduction

Bitline multiplexers (column multiplexers) are used to transfer the data contents from a selected set of bitlines to the I/O-port (see Fig. 2.1, Fig. 2.3). An important issue is the position of these multiplexers [38]. If they are placed behind the sense amplifiers, each column requires one amplifier. This increases power dissipation and area. In order to match the pitch of the sense amplifiers with the bitline pitch, the sensing circuit must be very simple. Therefore in many SRAM designs the multiplexer (MUX) is located between the columns and the sense amplifier as shown in Fig. 5.1 (see also Fig. 2.3). The advantage is that more area can be allocated per sense amplifier as only one sensing block is utilized to read out several multiplexed bitline pairs.

Unfortunately, column select transistors used as a switch in the bitline multiplexer are not ideal switches. Their finite on-resistance adds to the low input resistance of the current sense amplifier and results in a significant performance degradation as will be investigated in this chapter. This is a main limitation of current sense amplifiers in today’s applications. As the multiplexer causes an additional RC delay [38], also voltage sense amplifiers are affected but less severely. Due to power and reliability requirements the

![Diagram](image_url)

Fig. 5.1. Bitline multiplexer located between memory columns and sense amplifier
supply voltage is constantly decreasing. At the same time the finite resistance of the bitline multiplexer causes more and more performance degradation.

Shibata has discussed the influence of the multiplexer with focus on current sensing in [39]. It is pointed out that due to the resistance of the multiplexer the current signals decrease, the sensing delay increases and, finally, the merit of current sensing disappears. It has been mentioned in [39] that enlarging the MOSFET channel width is a way for reducing the multiplexer resistance but it increases area and parasitic capacitance. As a result, in [39] a scheme has been proposed where the read-out signals are multiplexed after sensing by a two-stage sense amplifier. The drawback is that the sense amplifier must fit into the pitch of the memory array.

Voltage sensing designs face the same difficulties. In [50] a faster bitline sensing is developed by eliminating the multiplexer at the local bitlines and placing it behind the sense amplifier. Several publications, e.g. [103], propose to increase the width of the bitline multiplexer to improve the delay.

An efficient solution to overcome the multiplexer influence has been presented by the author in [104, 105].

### 5.2 Analysis of the Multiplexer

#### 5.2.1 General Considerations

Sense Amplifier and multiplexer can operate as a current sink or as a current source (see Sect. 4.1, Fig. 4.1). Figure 5.2 shows the different structures where the n- and p-channel transistor represents one switch of the multiplexer. The sense amplifier is modeled by the small-signal input resistance $r_s$ and by the DC voltage $V_{ref}$ of the current sensing input stage. The input resistance refers to $Z_{BLS}(s = 0)$ for $r_{in} \rightarrow \infty$ while $V_{ref}$ is the extrapolated voltage at the input of the sense amplifier for zero input current (Chap. 4). Due to the well-defined potential it is not necessary to use a transmission gate (p- and n-channel transistor in parallel).

From Fig. 5.2 several rules can be derived. The voltage $V_{ref}$ in Fig. 5.2a and d and the bitline voltage $V_{BL}$ in Fig. 5.2b, c have to be chosen properly, so that the multiplexer transistor turns on completely ($|V_{GS}| > V_{th}$).

To save layout area the switches are usually not placed in separate wells and a bulk-source voltage $V_{BS}$ occurs. The body effect causes an increase in the threshold voltages $V_{thn}$ and $V_{thp}$, respectively.

Obviously, the output characteristics of the transistor defines the effective input resistance if the transistor’s drain is the input terminal as for the n-channel transistor in Fig. 5.2a and the p-channel transistor in Fig. 5.2d. To obtain a low input resistance the transistor always has to be biased in the linear region. In the second case (source at bitline, Fig. 5.2b, c), the bitline voltage influences both the gate-source and the drain-source voltage. In the saturation region the input characteristics of the MOS transistor becomes