Chapter 4
Multi-Gate Related Design Aspects

In this chapter analog and mixed-signal circuit design aspects related to multi-gate specific device behavior are discussed. The main goal is to provide an early, technology oriented circuit assessment, focusing on different variation aspects. Based on a close link to device and technology the feasibility of analog and mixed-signal circuits in emerging FinFET technologies is proven. Performance differences and advantages compared to planar CMOS are quantified with examples. The assessment covers a broad range of analog and mixed-signal circuits, starting from basic biasing blocks, over OpAmps to D/A converter and PLL as mixed-signal examples. An outlook to RF design aspects is given by the discussion of 2 GHz VCOs and LNAs. The final sections cover further design aspects related to the SOI FinFET device structure.

For all circuit simulations shown here a dedicated FinFET compact model is used [95]. The measurement results are obtained from FinFET devices as presented in Chap. 2 which are also used for model parameter extraction.

4.1 Biasing Circuits

Biasing circuits are key analog building blocks intended to generate and distribute stable reference currents and voltages, robust against variations of supply voltage and device parameters. Although also bandgap voltage reference circuits fit into this definition, they are covered in a separate section, since additional aspects such as p-n junctions and OpAmp design have to be considered.

4.1.1 Matching Optimized Current Mirrors

The current mirror is one of the most frequently used building blocks in analog circuits. Roughly speaking current mirrors are used to generate replica currents representing exact multiples of the input current, see Fig. 4.1(a). Deviations from ideal
current mirror behavior are caused by finite output impedance and device parameter mismatch in DC case. From AC perspective the constant bias voltage at the common gate is affected by output voltage variations which are AC coupled via the gate-drain capacitance. Thus, the devices should feature high output impedance and good matching at low area, i.e. low parasitic capacitances.

Obviously the low $g_{ds}$ of FinFETs directly corresponds to an improved output impedance resulting in lower sensitivity against output voltage variations, see Fig. 4.1(b). The advantageous matching behavior can be used to decrease area and improve AC performance compared to planar implementations.

As mentioned in Chap. 2 the matching of FinFETs is affected by several layout dependent effects. A current mirror test-structure with multiple outputs as shown in Fig. 4.1(a) is used to compare different FinFET specific layout styles in order to derive matching optimized layout guidelines [66].

The "golden rules" for good matching in analog layout can be summarized in few catchwords: symmetry, unit devices & cells and regular environment. Following these guidelines several different basic layout styles are possible, as illustrated in Fig. 4.2:

- **Shared source/drain areas (A):** Each current mirror device is splitted into several unit devices with equal fin count and merged source/drain landing pads. Dummy gates are placed to ensure regularity. The current flows in anti-parallel directions.
- **Shared source/drain areas with dummy fins (B):** Same layout as (A) with additional dummy fins to improve regularity and to avoid contribution of “outer” fins that do not match “inner” fins.
- **Single source area (C):** The current mirror devices are splitted into several unit devices. All devices share a common source landing pad, i.e. gate misalignment affects all devices in the same way. The current flows in only one direction. Dummy devices improve regularity.