This chapter presents a method to enhance the performance of a time-interleaved ADC, using the open-loop T&H circuit introduced in Chapter 7. The approach is able to measure the mismatches between the various channels of a time-interleaved system on-chip, and to correct for these imperfections by means of analog calibration. The calibration method will be discussed, and both simulation results and experimental results will be shown. Parts of this chapter have been published previously in [77, 78].

1. Introduction

Time-interleaving multiple analog-to-digital converters (ADCs) [59] is a widely used approach to accommodate the demand for higher sampling rates combined with high accuracy and low power consumption. For example, in Fig. 9.1, $p$ parallel ADCs, each with a separate track-and-hold (T&H) circuit, are combined to compose a $p$ times faster ADC: each T&H samples the same input signal $V_{in}$ with the same sample rate $f_s$, but the samples are taken at different phases of the clock, such that after digital recombination, the overall system behaves as a single ADC operating at $f_s$. In this work, the combination of a single T&H and a single ADC will be called a channel; i.e. the complete ADC is then composed of $p$ channels. Apart from the architecture in Fig. 9.1, where each channel contains its own T&H, there are also alternative solutions like using one dedicated T&H in front of all channels. However, this work focusses on the architecture of Fig. 9.1, which is a commonly used solution.

The accuracy of a time-interleaved ADC is limited by two properties, namely: the accuracy of the individual channels that compose the time-interleaved ADC, and the matching accuracy between the channels. When the open-loop T&H as presented in Chapter 7 is to be used in a time-interleaved converter, both the accuracy of each individual T&H and the matching between
several T&H’s has to be taken into account. The first requirement can be fulfilled by the calibration method presented in Chapter 8. Therefore, this chapter focuses on the calibration of the matching errors between the T&H channels. In practice, a combination of both calibration methods could be implemented to correct for both the errors of the individual channels and the errors between the different channels. However, this combination is beyond the scope of this work.

There are many effects that result in matching errors between the ideally identical channels, for example:

- Random mismatch of components (transistors and capacitors) in the channels and the clock circuitry.

- Systematic mismatch of components due to gradients on the die, affecting the channels differently.

- Timing mismatches due to differences in wiring and capacitance in the common clock circuitry and input network.

- Common-mode and power supply gradients due to differences in DC paths.

As all these problems are dependent on the architecture of the channels, the transistor-level design, the technology properties and the actual layout, it is difficult to derive an exact model of the mismatch errors. Instead, it is common practice to use an abstract model to represent the mismatch errors. The most widely used and accepted model considers three mismatch errors: offset, gain error and time-skew [60]. On system-level, this error-model can be used to derive mismatch requirements based on the final accuracy target. Then, during the design and implementation of the ADC, the actual errors can be translated to this simplified model and verified accordingly.