Chapter 6

ΣΔ Modulator Robustness

In the analysis of the ΣΔ modulator’s algorithmic accuracy in Chap. 5, the circuits are assumed to have no imperfections. In reality, the performance of the circuits will come at the cost of resources (area and power). Trade-offs have to be made to come to a good performance-to-resource ratio which can be verified in a benchmark with other ΣΔ modulators. The benchmarking of modulators will be done in Chap. 8. In this chapter, the relation between architecture choices and circuit imperfections and their impact on the ΣΔ modulator performance and cost will be discussed. The subjects of discussion are:

- Technology
- Continuous-time vs. discrete time loop filter
- Feed-forward vs. feedback loop filter
- Gain accuracy
- Circuit noise
- Linearity
- Aliasing
- Excess loop delay
- Clock jitter

A schematic overview of the above is presented in Fig. 6.1. The block diagram on the bottom of Fig. 6.1 illustrates all relevant imperfections for a continuous-time ΣΔ modulator which will be discussed in this chapter. In this chapter, first it will
be explained why it is advantageous, to replace analog circuits by digital circuits where possible. As analog IP will never be completely digital, the most robust architecture for remaining analog functions should be searched for. In this chapter, the latter is done for $\Sigma\Delta$ modulators. The focus will be mainly on $\Sigma\Delta$ modulators with a 1-bit feedback DAC, as most of the implementations presented in this book have a 1-bit feedback DAC (one implementation has a 1.5-bit feedback DAC). Where relevant, modulators with multi-bit DACs will be discussed.

### 6.1 Portable, Technology Robust Analog IP and Time-to-Market

The quest to increase digital processing per unit area has led to scaling of CMOS technologies, yielding faster and smaller transistors. In [4] the technology scaling factor $s_T$ is introduced to investigate the impact of technology scaling on digital circuits. The technology scaling factor $s_T$ is defined as the ratio between the minimum L of a transistor in the current technology node and the minimum L of the previous IC technology node or $s_T = \frac{L_{\text{min, current node}}}{L_{\text{min, previous node}}}$ and is approximately 0.7.