Molecular filter-nanosieve

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Abstract

Demonstrated in this paper is a molecular sieve. The focus of this work is making a “smart” filter. This filter has electrochemical and electromechanical properties that would allow both sorting and filtering of solutions. Prior sifters and sieving structures have been at the mercy of a static material structure, whereas the convention proposed here allows dynamic control of filtering size during an assay.

The filter mechanism simply relies on a sandwiched layer of oxide, grown in a RF Sputtering system. This allows for almost Angstrom level control of the thickness. An oxide layer is sandwiched between two layers of silicon with e-beam written holes 100nm in diameter, one offset from the other. Dry etching is used to carve these holes in the silicon layers, and wet oxide etching defines a void in the sandwiched layer. The distance that the two silicon layers are separated dictates the smallest filtering size.

Analysis is available through several methods. Mechanically, a fluid can be passed through the holes carrying along with it the particles or molecules that are small enough to make it through the oxide layer. Electrochemically, a charged particle can be placed on one side of a container and separated by the filter, while having the tendency to get to the other side, with different concentration, by passing through the filter [1].

Keywords: microfluidic, filter, sieve, molecular, nanopore, nanofluidic

1. Introduction

The analysis of small volumes of solutions is extremely important for many biological applications. The goal of this work is to define small cavities that can be used to filter sub-100 nm particles and even molecules. Here we present the design and fabrication details of such filters, as well as preliminary experimental results.

2. Theory

Sputtering and etching are common processes that are used in microelectronics microfabrication, but can be applied to the nanofabrication of fluidic devices. Using these processes for new areas offers the opportunity for combining the excellent dimensional control from the microelectronics industry with the massive integration of miniaturized devices on a monolithic substrate. That is why we seek to fabricate our nanosieve lithographically. However, even with the excellent capabilities of high-resolution lithography, it is very difficult to define hole sizes below 10 nm with adequate uniformity for high quality filtration. Therefore, it is desirable to define filters in which the geometric size of the constriction is controlled by growth rather than by lithography. Here we demonstrate such a geometry, in which we use the vertical control over layer thickness to determine the filter size, and provide access to this constriction by

lithographically defined holes. To define the filter, we use two steps of electron beam lithography and dry etching with multiple alignments to obtain off-set holes within two thin silicon membranes, which are connected through a sacrificial silicon dioxide layer that ultimately controls the filter size. Since the layer thickness of a sacrificial layer can be controlled to within less than 1 nm during the construction of the filter, it is possible to accurately set the filter geometry and control the size of particles or molecules that can pass through the filter.

![Figure 1. Illustration of nanosieve, left, and close-up on the right, with a thin gold film evaporated on both sides of the substrate. (Layers not drawn to scale.)](image)

3. Experimental

The fabrication sequence is summarized in Figure 1, where we show the steps which are needed for defining our lithographic filter. First, we use electron beam lithography to define an array of holes on a silicon on insulator (SOI) sample. The thickness of the silicon layer is approximately 200 nm, whereas the SOI oxide thickness is approximately 400 nm. We use polymethylmethacrylate (PMMA) as an electron beam resist, as well as an etch mask. Using a chemically assisted ion beam etching system (CAIBE) with XeF2 reactive gas, the pattern written using e-beam lithography, illustrated in Figure 2, is etched through the first silicon layer. The beam voltage and other parameters are set appropriately in order to maintain an acceptable etch ratio between the etch mask layer and the silicon. Following this procedure, the etched holes are filled with gold, and the PMMA is removed in acetone. Then, a precisely controlled silicon dioxide sacrificial layer is sputtered onto the sample, followed by a thicker polycrystalline silicon layer. Another lithography procedure is then used to define a similar array of holes, with a small offset, on top of the original hole structure. Finally, hydrofluoric acid and gold etch are used to define the connection between the lithographically defined holes through the silicon dioxide sacrificial layer.

![Figure 2. SEM view of e-beam written, etched holes and alignment mark used for offsetting the top layer.](image)

![Figure 3. Suspended epi-Si membrane with e-beam written holes in the center.](image)