Features of a Scan and Clock Resource Chip for Providing Access to Board-Level Test Functions*

BULENT I. DERVISOGLU
Hewlett Packard/APOLLO, 300 APOLLO Drive, Chelmsford, MA 01824

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Abstract. The architecture and some of the specific features of a Scan and Clock Resource (SCR) chip are described. This chip is currently being used in a high-end workstation product to provide access to the testability features of the individual chips and/or printed circuit boards. Using a board-level controller to gain access to the testability features of system components and interfacing the controller to a diagnostics processor (or external tester) is emerging as a common strategy for designing testable digital systems. Based upon experience gained from such an application, controller features that are deemed useful are discussed.

Key words: boundary scan, design-for-testability, diagnostics bus, pseudorandom testing, scan.

1. Introduction

Scan-path technology, which originated more than 15 years ago, has finally become the method of choice for implementing Design-for-Testability (DFT) features in complex integrated circuits and systems. Provided that the circuits have been designed with adequate DFT features to allow test patterns to be developed, testing of individual chips on specialized Automatic Test Equipment (ATE) can be achieved in a straightforward fashion due to the accessibility of chip pins by the ATE. This allows test patterns to be stored and applied to the Circuit-Under-Test (CUT) using the hardware and software capabilities of the ATE.

As we move through the levels of test hierarchy, in-circuit testing using a bed-of-nails structure is a presently popular approach to testing populated circuit boards. However, it is becoming increasingly desirable to perform board-level testing without using a specialized in-circuit tester. This requires replacing the in-circuit tester with a centralized resource to control the board-level test functions. Testing of populated circuit boards poses problems due to the inaccessibility of individual chip pins as well as problems associated with keeping certain areas of the board logic unaffected by the test activity that may be present in other areas. In an effort to address the board-level test problems several standardized circuits have been proposed for use as a common resource to be included on every Printed Circuit Board (PCB) and link that PCB to an internal or external test processor. One of the earlier approaches has been the TURINO circuit [1] which defines a TESTABILITY BUS and an associated component that connects to the testability bus in order to provide board-level controllability/observability signals. This circuit makes no assumptions about the testability features supported by the components present on the PCB. To use this approach, first the test engineer is required to analyze the board-level logic and determine where test points (signals) should be defined and use the board-level control resource(s) to provide the necessary signals and/or observe their values. A different circuit is described by Breuer and Lien [2] in which a Module Maintenance and test Controller (MMC) is presented as a flexible and programmable central resource capable of controlling both the VHSIC ETM-BUS [3] and the IEEE 1149.1 BUS [4] and report the test results to the external test processor using the TM__BUS [5]. Whereas this proposal focuses on the interface to the various buses it does not specifically answer board-level test issues and how this module may be used to solve them. Another similar chip was proposed by Ballew and Streb [12] in order to gain observability of board-level signals.

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One of the most significant developments in the test area have occurred recently with the acceptance of the 1149.1 Test Access Port as a boundary scan standard by the IEEE [4]. Among the companies who announced support for this approach is Texas Instruments which also announced some board-level components for controlling chips that comply with the IEEE 1149.1 standard. In particular, TI announced SCOPE testability controllers [6] that allow multiple scan paths to be connected together (e.g., ACT8997/8999 Scan Path Selectors) or generate IEEE 1149.1 protocols from interfaces to 16-bit microprocessors (e.g., ACT8990 Test Bus Controller). TI’s SCOPE family of testability components are designed to make it possible to build a test architecture made up of IEEE 1149.1 compliant ICs but do not specifically address problems present in testing PCBs that contain components that implement different (or none at all) testability standards.

Rather than requiring an entire PCB to be in full compliance with some generally preferred testability standard, it is more realistic to expect that some of the board-level components shall have different or no test features. Nevertheless, it is necessary to be able to control all of the board-level test features from a central resource which should be flexible enough so it may be adapted to different environments/requirements. This paper describes the scan and clock resource (SCR) chip used as the board-level controller in the APOLLO DN10000 workstation [7]. It will be shown that by identifying the key differences in the features of the board-level components it was possible to select certain differences to be handled directly by the SCR (i.e., in hardware), whereas others have been left to be resolved by the diagnostics software. This way, it has been possible to present a homogeneous view of all system boards to the service processor which contains the intelligence to perform the necessary test/diagnostics functions during manufacturing as well as field testing of the DN10000.

2. The Scan and Clock Resource (SCR) Chip

The APOLLO DN10000 workstation uses individual SCR chips on each system board. The SCR is responsible for generating the various clock signals as well as providing access to the scan paths and other testability features that may be present on that board. Each SCR chip can handle up to 8 independent ports, and supplies the scan control and functional clock signals for each port separately. The clock control circuitry inside the SCR has been carefully designed to minimize the skew among the multiple copies of the clock signals that it generates. Different boards have their clocks aligned with respect to each other using a local voltage-controlled crystal oscillator (VCXO) and a phase-locked loop. A free-running version of the clock outputs from the SCR is used to provide its own clock, as shown in figure 1.

Each SCR also interfaces to a system-wide Diagnostics Bus (DBUS) in order to be able to communicate with the service processor which always acts as the bus master. The DBUS is a serial bus that comprises signal lines clock, valid, cmd, data_to_SCR,