Transient Capacitance Measurements of Interface States on the Intentionally Contaminated Si–SiO$_2$ Interface

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Abstract. The constant capacitance transient capacitance technique (CC–DLTS) was applied to analyse the effect of impurities on MOS interface states. The elements Cs, Pb, Xe were ion implanted prior to oxidation. Sodium was implanted directly into SiO$_2$ and drifted to the interface. The alkali ions cause a steep increase in the density of interface states near the conduction band edge. The other elements studied show little effect on the interface properties. The capture cross-section for electrons decreases strongly near the conduction band.

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We have studied the effect of impurities on density and properties of MOS interface states. The influence of impurities in semiconductor insulator interfaces is not well understood, but it is expected that impurities have a strong effect since in recent years the density of states in MOS interfaces could be markedly reduced by improvement of cleanliness standards.

Ion implantation was used to introduce the impurity into the MOS interface for the study using the same technique, as previously published [1]. Ion implantation makes it possible to select special types of elements with high purity and to incorporate these elements directly into the interface in a controlled manner by choosing the appropriate energy. In order to avoid radiation damage in the interface we implant the impurity under consideration before oxidation into the bare silicon surface with a well controlled dose of the order $10^{12}$–$10^{14}$ cm$^{-2}$. The silicon wafer is then oxidised thermally with standard technology to obtain approximately 1000 Å thin SiO$_2$ layers. It is known that during formation of the oxide from the implanted Si-layer, the impurity redistributes itself to establish an equilibrium with the interface. As indicated in the schematic drawing of Fig. 1, most impurities are gettered in the interface region. A concentration profile with peaks in the interface and at the surface is generally observed by secondary ion mass spectroscopy SIMS [1, 2].

![Fig. 1. Schematic drawing of the procedure to introduce an implanted impurity into the MOS interface](image-url)
The new feature of the present paper is the application of the transient capacitance measurement technique DLTS to analyse the dynamic properties of MOS interface states in presence of impurities. The DLTS technique has been mainly used to measure bulk defects [3–5]. It has also been successfully applied to study MOS interface states in the case of state-of-the-art clean MOS interfaces [6–8]. The technique features high sensitivity and complements the conventional techniques, e.g. the quasistatic and conductance technique for measuring interface state properties, in that it is not affected by surface potential fluctuations which arise from the random spatial distribution of fixed positive charge in the oxide. The technique is therefore especially advantageous for measuring interface states at energies close to the band edge.

Details on the measurement technique and the evaluation analysis are given elsewhere [9]. Here we only explain the main details of the measurement procedure and evaluation. New results are shown for the interface state density distribution in presence of the alkali elements Cs and Na in the interface region. These elements are known to have a critical effect on the fixed interface charge. We could show that these impurities also have an effect on the fast interface state density close to the band edges. This region is not accessible to the conventional measurement techniques. Results for other contaminants, e.g. Pb and Xe, which mainly cause radiation damage are also shown. The experimental results are discussed in the light of theoretical models for MOS interface states.

**DLTS-Measurement on MOS Structures**

The measurement principle is explained in Figs. 2 and 3. During a 20 μs pulse the MOS capacitor is biased into accumulation to fill all interface traps with majority charge carriers, e.g. in our case electrons. During the pulse interval the bias voltage is adjusted so that the Fermi level in equilibrium is located in a midgap position. The change of the interface charge is monitored by measurement of the MOS capacitance. As indicated in Fig. 3, we use a feedback from the capacitance bridge to the bias power supply to maintain a constant capacitance. The relaxation of the interface charge is then monitored by the bias voltage. The change of the gate voltage required to maintain a constant capacitance appears only across the oxide layer. The interface charge change per unit area AQss(t) which is proportional to the interface state density therefore is simply related to the observed gate voltage signal AV(t) by

\[ AV(t) = \frac{\Delta Q_{ss}(t)}{C_{ox}} \]

where \( C_{ox} \) is the oxide capacitance and \( \Delta \) the capacitor metal gate area. It is assumed that during the pulse interval interface states emit the trapped charge by thermal emission \( \sim \exp(-t/\tau_e) \) with time constant

\[ 1/\tau_e = \sigma v_{th} N_c \exp(-E/kT) \]

where \( \sigma \) is the capture cross-section and \( v_{th} \) the thermal velocity of electrons, \( N_c \) the effective density of states in the conduction band, and \( E \) the energy depth of the interface state below the conduction band edge. As indicated in Fig. 3, the gate voltage \( V_G \) is sampled at two different delay times \( t_1 \) and \( t_2 = 2t_1 \) and the difference signal

\[ AV_G = V_G(t_1) - V_G(t_2) \]

is formed in the DLTS measurement. For electron emission from a continuous distribution of interface traps, we obtain for the DLTS signal \( AV_G \) from (1)–(3)

\[ AV_G = A/C_{ox} \int qN_{ss}(E) \exp(-t_1/\tau_e) - \exp(-t_2/\tau_e) \] dE.

Fig. 2. Schematic drawing to illustrate the measurement principle of DLTS applied to an MOS structure

Fig. 3. Schematic drawing to explain the correlation procedure in the "Constant Capacitance Transient Spectroscopy" CC-DLTS