The operation of a digital-analog converter can be represented by equation

\[ U_{\text{out}} = AED, \]  

where \( U_{\text{out}} \) is the output voltage, \( A \) is a scale coefficient, \( E \) is a stable reference voltage, \( D \) is a proper fraction subject to conversion.

\[ 0 < D < 1. \]  

\[ U_{\text{out}} = AE \] for \( D = 1. \)

The converted figures are usually represented by positional number systems. In such systems the \( n \)-order \( p \)-digit fraction has the form of:

\[ D = a_1 \cdot p^{-1} + a_2 \cdot p^{-2} + \ldots + a_n \cdot p^{-n}, \]

where \( p \) is the base of the number system, \( a_i \) one of the possible symbols of the \( i \)-th order.

If the fraction meets condition (2) then

\[ a_i = 0; 1; 2; \ldots; p - 1, \ i \neq n; \]

\[ a_n = 0; 1; 2; \ldots; p. \]

A digital-analog converter which corresponds to this method of representing numbers has a multiorder structure. A circuit representing a single order we shall call in future a location.

This article deals with converters whose locations consist of discrete voltage-divider circuits with a constant output resistance. In [1] such converters are defined as parallel voltage converters or voltage converters of the \( E_2 \) type.

The voltage converter location (Fig. 1a) consists of elements \( G_1 \) and \( G_2 \), and it has an output conductance \( G_{\text{out}} = G_1 + G_2 \) and an output voltage of

\[ U_{\text{out}} = \frac{G_1}{G_1 + G_2}. \]

A constant output conductance is provided by the circuit of Fig. 1b which contains sets of conductances and throw-over switches [1, 2]. If \( g_s \) is a single conductance of such a divider, we find that:

\[ G_1 = xg_s; \]

\[ G_2 = (Q - x) g_s, \]

\[ G_{\text{out}} = Qg_s, \]

where \( x \) is the number of unit conductances connected to bus \( E \); \( Q \) is the total number of unit conductances in a location set.

A shunt conductance \( g_{\text{sh}} \) connected to the output terminals changes the scale of the output voltage and total conductance of the location:

\[ U_{\text{out}} = \alpha \cdot E \cdot \frac{x}{Q}, \]
\[ G_{\text{out}} = \frac{G_{\text{out}}}{\alpha} = \frac{Q \cdot G_{s}}{\alpha}, \quad (7) \]

\[ \alpha = \frac{G_{\text{out}}}{G_{\text{out}} + G_{\text{sh}}} < 1. \quad (8) \]

It is essential that
\[ Q = x_{\text{max}} \quad (9) \]

Let us derive an expression for the voltage at the apex of the star formed by several, in a general case shunted, locations which use a common reference voltage \( E \) (Fig. 2):

\[ U_{\text{out}} = \frac{\alpha_{1} x_{1} G_{\text{out}1} + \alpha_{2} x_{2} G_{\text{out}2} + \cdots + \alpha_{n} x_{n} G_{\text{out}n}}{\sum_{i=1}^{n} G_{\text{out}i}}. \quad (10) \]

Formula (10) contains in an implicit form an expression for an \( n \)-order \( p \)-digit fraction of the type of (3), if it is assumed that \( x_{i} = a_{i} \). Then according to (9) and (4) we find that
\[ Q_{i} = p - 1, \quad i \neq n; \quad Q_{n} = p. \quad (11) \]

Let us transform expression (10) by taking into account (11) and introducing notation
\[ \beta_{i} = \frac{G_{\text{out}i}}{G_{\text{out}1}} \quad (12) \]

As a result we obtain the basic equation for an \( n \)-order \( p \)-digit digital-analog converter with a constant output resistance:

\[ U_{\text{out}} = \frac{p}{(p - 1)} \left[ \frac{\alpha_{1} \beta_{1}}{p} x_{1} + \frac{\alpha_{2} \beta_{2}}{p} x_{2} + \cdots + \frac{\alpha_{n} \beta_{n}}{p} (p - 1) x_{n} \right]. \quad (13) \]

The output conductance of the converter is:
\[ G_{\text{out}} = \sum_{i=1}^{n} G_{\text{out}i} = G_{\text{out}1} \cdot \sum_{i=1}^{n} \beta_{i}. \quad (14) \]

Equation (13) coincides with (1) provided that
\[ A = \frac{p}{(p - 1) \sum_{i=1}^{n} \beta_{i}} \quad (15) \]

and
\[ D = \frac{\alpha_{1} \beta_{1}}{p} x_{1} + \frac{\alpha_{2} \beta_{2}}{p} x_{2} + \cdots + \frac{\alpha_{n} \beta_{n}}{p} (p - 1) x_{n}. \]