A Switch-Level Test Generation System for Synchronous and Asynchronous Circuits

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Abstract. A switch-level test generation system for synchronous and asynchronous circuits has been developed in which a new algorithm for fully automatic switch-level test generation and an existing fault simulator have been integrated. For test generation, a switch-level circuit is modeled as a logic network that correctly models the behavior of the switch-level including bidirectionality, dynamic charge storage, and ratioed logic. The algorithm is able to generate tests for combinational and sequential circuits. Both nMOS and CMOS circuits can be modeled. In addition to the classical line stuck-at faults, the algorithm is able to handle stuck-open and stuck-closed faults on the transistors of the circuit.

In synchronous circuits, the time-frame based algorithm uses asynchronous processing within each clock phase to achieve stability in the circuit and synchronous processing between clock phases to model the passage of time. In asynchronous circuits, the algorithm uses asynchronous processing to reach stability within and between modules. Unlike earlier time-frame based test generators for general sequential circuits, the test generator presented uses the monotonicity of the logic network to speed up the search for a solution. Results on benchmark circuits show that the test generator outperforms an existing switch-level test generator both in time and space requirements. The algorithm is adaptable to mixed-level test generation.

Keywords: Automatic test generation, reverse time processing, sequential circuits, stuck-open and stuck-at faults, time-frame expansion.

Introduction

Research in switch-level test generation can be classified according to several methods. One class of algorithms includes methods that have implemented existing gate-level test pattern generators to detect transistor stuck-open faults [12, 13]. While these methods are limited to combinational circuits they have attempted to model the potential sequential nature of the circuit in the presence of a stuck-open fault. Various circuit characteristics and properties of the switch-level are not modeled.

Another class of algorithms has dealt directly with the switch level [1, 8, 11, 18]. In addition to being limited to combinational circuits, these algorithms were also restricted in the switch-level aspects that could be handled. These algorithms can exhibit poor performance due to the exponential growth of the number of possible paths between a module's output and power terminals. To reduce the complexity, Lioy [15] developed a mixed-level test generator which expands only the faulty block to the switch-level. The non-faulty portion of the circuit is processed at the gate level. His algorithm generates tests only
for combinational circuits. Of these algorithms, only [8] reports an implementation and provides performance data on small circuits.

Recently, Cho and Bryant [9] have developed a test generation algorithm based on Bryant's switch-level simulator COSMOS [5], and have reported successful test-pattern generation for circuits with up to 770 transistors. While it improved upon previous test generators, their test generator suffers from excessive dynamic memory requirements. In addition, the amount of user intervention is also significant for large circuits. Reddy [17] has also implemented a sequential test generation algorithm for MOS faults. In his algorithm, he used the switch-level model of Bryant's MOSSIM-II simulator [3] and PODEM [11]. Another recent switch-level test generation system was implemented by Lee [14]. His test generator was based upon PODEM and was able to handle bridging faults in addition to line stuck-at and transistor stuck faults.

Several mixed-level test generators have also been developed recently. In its capabilities to handle a mixed gate and switch-level sequential circuit, the promising mixed-level sequential test generator of Chen and Abraham [7] comes closest to that described in this paper. However, it applies a nine-valued relaxation algorithm to strongly connected DC coupling components whereas we use a gate-level representation of the switch-level circuit and optimize the time-frame based approach for test generation. Their test generator also performs current testing to detect faults that are aborted or undetectable by logic tests.

The simulation-based mixed-level test generator developed by Saab, et al. [19] continuously alters a given test vector sequence to obtain new test vectors for stuck-at and transistor faults. The new test sequence is then applied to a fault simulator. The fault coverage results reported for their test generator were not as good as other gate-level and switch-level test generators. Another mixed-level test generator was developed by Gläser, Vierhaus, and Hübner [20]. Their FAN-based algorithm performs test generation at the gate-level for combinational and sequential circuits. It obtains tests at the switch-level by providing an interface to the CTEST switch-level test generator. Their test generator is applicable to current testing as well.

A neural network approach for testing stuck-open faults has been proposed recently [21]. The new algorithm is restricted to combinational circuits and would require neural network hardware or parallel computation to be efficient.

At the same time that VLSI circuits continue to become more complex and transistor densities continue to increase, integrated circuit manufacturers are demanding higher quality. As a result, testing has become an integral component in the design and manufacturing process. Testing of sequential circuits and testing for stuck-open faults remain as critical problems. Presently, few switch-level test generators have been implemented and proven useful commercially. While switch-level testing offers a possible solution to a number of problems, mixed-level testing may provide a more viable alternative.

This paper presents an update to a previous paper [10] describing an algorithm and the implementation of a Switch-LEVEL TEst generation system (SVELTE). Features of the algorithm include the ability to handle sequential as well as combinational circuits; the ability to handle both synchronous and asynchronous circuits; the ability to handle both line stuck-at faults and transistor stuck-open faults; fully automatic processing; reverse time processing to generate the final test pattern first, followed by the generation of any initial test patterns that are necessary; and a combination of search-based techniques with some symbolic processing. The algorithm currently has some mixed-level capabilities and is easily extendible to a complete mixed-level test generation system.

Circuit and Fault Model

We model a circuit at two levels; a network of logic gates describing the behavior of each module locally and an interconnection of modules describing the circuit behavior globally. In general, the module-level network is an asynchronous sequential circuit capable of modeling the aspects of switch-level behavior important to fault modeling and test generation. This includes memory states (stored charge) under