The binary notation of the symbols of a subcode consisting of permutation words of a code $K$ over $GF(2^m)$ will generate a binary code with a constant weight of length $n = m^2 m$ and a number of "ones" equal to $n/2$. It is well known [8] that the frequency spectra of such codes have a shape that is suitable for signal transmission, i.e., the level of the constant component is either fixed or equal to zero, and there is no random component of the spectrum at the clock frequency, as a result of which clock synchronization is simplified and the noise immunity is increased; the amount of energy in the lower part of the spectrum is limited, and hence there is higher stability of the signal with respect to impulse noise which is most hazardous at low frequencies, for example in cable transmission lines.

These properties of the codes considered above and the availability of a simple error correction procedure for them make these codes very suitable for use in digital data exchange lines.

The author expresses his gratitude to V. S. Kogan for useful remarks.

LITERATURE CITED

3. É. L. Blokh and V. V. Zyablov, Generalized Cascade Codes [in Russian], Svyaž', Moscow (1976).
6. B. M. Zlotnik, "An algorithm of numeration of the Mathieu groups $M_{11}$ and $M_{12}$, and error correlation in codes equivalent to these groups," Kibernetika, No. 1, 40-44 (1978).

SYNTHESIS OF MONITORING DEVICES FOR DIGITAL AUTOMATA

A. M. Smirnov

Discrete systems composed of functionally related replaceable units are frequently required to monitor their performance continuously and automatically and to diagnose their faults in the course of operation to within a single replaceable unit. A replaceable unit in this case is a device which can be represented by a digital automaton (DA) or a combination of such automata. The term replaceable denotes the possibility of replacing the faulty unit manually by the operator or the possibility of automatically connecting a similar unit if the system is provided with redundancy. In addition to test diagnosis, such requirements are satisfied by the addition of hardware monitoring of DAs [1-3]. Each replaceable unit is provided in this case with a monitoring device (MD) which continuously monitors its performance and generates a signal if the given unit fails. The feasibility of using such methods depends on a successful solution of the problem of MD minimization.

Most works, in particular [1-3], propose methods of synthesizing and minimizing MDs treated as independent devices, i.e., without taking into account the input and output relations of the monitored automaton with other DAs composing the system.

A method has been proposed, e.g., [4], for synthesizing MDs for a group of digital automata forming a chain whose links also are digital automata. In such a chain the inputs of any link, i.e., of a DA, are connected to the outputs of an adjacent link. In this method the check outputs of each link are produced so that an error in the input vector causes an error in the output vector. The input and output vectors of a link contain both data and check bits. Thus, in each link the check bits of the output vector can be generated from the

check bits of the input vector which simplifies the circuit (encoding automaton) which generates these bits. Moreover, the entire chain requires only one device (decoding automaton) which monitors the presence of an error in the output vector of the last link of the chain.

Since any discrete system can be represented as an assembly of chains, possibly more complex than in [4], in synthesizing the MD of the system we will apply this method provided the chains belong to one replaceable unit. The method does not diagnose faults of the discrete system if the chain links belong to different replaceable units since an error in the output vector of one link causes errors in the output vectors of all subsequent links.

Here we propose a technique for synthesizing and minimizing MDs of DA groups forming chains, automata comprising the links of one chain belonging in the general case to different replaceable units. The MDs synthesized by this method ensure the detection and, with a given probability, the diagnosis of faults to within one link of the chain, i.e., to within one digital automaton, and consequently, to within one replaceable unit of the discrete system over a time not exceeding the permissible time. The method is based on the probability distribution of faults and of the set of input vectors of the chain DAs and also on the use of the output vectors of the encoding device of the preceding link as input vectors of the encoding device of a succeeding link. The problem of synthesis and minimization of MDs is formulated and solved using as an example a simple chain, but the solution technique is applicable to practically all chains.

Problem Formulation

Let a chain (Fig. 1) contain f links each of which includes a DA and also encoding and decoding automata (ENA and DEA). The latter make up the monitoring device (MD) which monitors the link and generates a signal \( \mathbf{S} \) when the link, i.e., the DA fails. The output vectors \( Y_{iDA_i} \) and \( Y_{iENA_i} \) of link \( i \) \( (i = 1, f - 1) \) of a chain are input vectors of \( DA_{i+1} \) and \( ENA_{i+1} \), respectively, of link \( (i+1) \). The vector \( X \) at the input of \( DA_i \) and \( ENA_i \) changes at the instants 1, 2, 3, ..., \( n \), .... The time interval between two consecutive instants is called a cycle. Assume that the probability \( P_X \) of the presence of some vector \( X \) for one cycle at the \( DA_i \) and \( ENA_i \) inputs is constant in time and independent of the form of \( X \) at the preceding cycles. The same properties are then true for the vectors \( Y_i \) and \( Y_{iENA_i} \) \( (i = 1, f) \) and the operation of each DA of the chain can be regarded as a Markovian process.

To the Boolean function implemented by \( DEA_i \) \( (i = 1, f) \) correspond the subsets \( CA_i \) and \( CV_i \) of the vectors \( (A_i, A_{iENA_i}) \) and \( (Y_i, Y_{iENA_i}) \) such that

\[
\begin{align*}
\forall (A_i, A_{iENA_i}) & \in CA_i \land \forall (Y_i, Y_{iENA_i}) \in CV_i, \quad \mathbf{S}_i = 0, \\
\forall (A_i, A_{iENA_i}) & \notin CA_i \lor \forall (Y_i, Y_{iENA_i}) \notin CV_i, \quad \mathbf{S}_i = 1,
\end{align*}
\]

where \( A_i \) is the \( DA_i \) memory state vector and \( A_{iENA_i} \) is the \( ENA_i \) memory state vector.

Further, let \( DA_i \) contain \( d \) binary logic elements each of which can have constant 0 (1) faults at the inputs and output. The total number of possible constant faults of the \( DA_i \) is \( N_f \). A constant error occurs when the characters of the function or formula implemented by a logical element are fixed at 0 (1).

Let \( P_{Yi-1} \) denote the probability of the vector \( Y_{i-1} \) being present at the \( DA_i \) input for one cycle. The operation of \( DA_i \) with a constant fault \( j \) \( (j = 1, N_f) \), provided that in each cycle \( (A_i, A_{iENA_i}) \in CA_i \) and \( (Y_i, Y_{iENA_i}) \in CV_i \), can be represented by the transition probability matrix

\[
P_j = \begin{bmatrix}
P_{11} & P_{12} & \ldots & P_{1m} \\
P_{21} & P_{22} & \ldots & P_{2m} \\
\vdots & \vdots & \ddots & \vdots \\
P_{m1} & P_{m2} & \ldots & P_{mm} 
\end{bmatrix},
\]

where \( m \) is the number of \( DA_i \) states in the absence of faults. The element \( P_{uv} \) \( (u, v = 1, m) \) of the matrix \( P_j \) is equal to the sum of the probabilities \( P_{Yi-1} \) of the vectors \( Y_{i-1} \) which transfer the automaton from state \( u \) to state \( v \). Only those vectors \( Y_{i-1} \) are considered for which

\( (A_i, A_{iENA_i}) \in CA_i \), \( (Y_i, Y_{iENA_i}) \in CV_i \),