High-Gain GaAs MESFET Op Amp

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Abstract. A gain enhancement technique for GaAs MESFET op amps is presented. It uses positive feedback to cancel the output conductance between the driver and active load transistors in a common-source amplifier configuration. An op amp using this technique was implemented in a 1-µm non-self-aligned GaAs MESFET process. The op amp exhibited a dc gain of 60 dB and a unity-gain frequency of 840 MHz.

1. Introduction

GaAs MESFET technology has for many years been extensively used in high-speed digital and microwave integrated circuits. The main advantage of GaAs over Si is its higher electron mobility and drift velocity. On the other hand, some deficiencies in GaAs technology have limited its application, especially in analog signal processing. One of the main limitations in GaAs technology is that GaAs n-channel MESFETs have an inherently low output impedance at high frequencies due to the presence of deep-level traps at the interface between the channel and the semi-insulating substrate. This has resulted in relatively low GaAs operational amplifier gain. Some gain enhancement techniques [1–6], which use either novel circuit design techniques or advanced GaAs technology, have been developed to increase the output resistance of active loads and boost the op amp gain.

In this paper, an alternative voltage gain enhancement technique and the design and implementation of an op amp using this technique are presented. The technique uses positive feedback to cancel the output conductance of the gain stage and achieve a high gain. The op amp using this scheme exhibits a high dc gain and a good bandwidth.

2. Conductance Cancellation Gain Enhancement Technique


In a basic GaAs gain stage, shown in figure 1a, the voltage gain is given by

$$\frac{V_o}{V_i} = \frac{-g_{md}}{g_{od} + g_{ol}}$$

where $g_m$ and $g_o$ denote the transconductance and output conductance respectively, and the subscripts $d$ and $l$ denote the driver and load devices respectively. Since the output conductance of a GaAs MESFET is large, the gain of a basic GaAs amplifier is limited.

From equation (1), it can be seen that high voltage gain results if the load conductance can in some way be manipulated until it becomes nearly the negative value of the driver conductance. This is the basis of the conductance cancellation scheme.

The matching negative conductance can be generated via positive feedback by connecting an amplifier with gain $A$ between the output node and the gate of the load transistor, as shown in figure 1b. In this configuration, the gain is given by

$$\frac{V_o}{V_i} = -\frac{g_{md}}{g_{od} + g_{ol}}$$

where the effective negative load conductance is

$$g_{ol}' = g_{ol} - g_{ol}(A - 1)$$
By choosing $A$ such that

$$A = \frac{V_x}{V_o} = 1 + \frac{g_{od} + g_{ol}}{g_{ml}}$$

(4)

then $g_{ol}$ would approximately cancel $g_{od}$ in equation (2), and the resultant voltage gain and output impedance can be very high.

2.2. Positive Feedback Realization

Figure 2 shows a gain stage implementing the conductance cancellation scheme. In this circuit, the basic DFET/DFET amplifier consists of $T_1$ and $T_3$, $T_2$ and $T_4$ are used to sense the output and feed it back to the load $T_3$. $T_5$ to $T_9$ function as a unity-gain inverter. Mixed-mode FETs (MFETs)\(^1\) are used for $T_2$ to increase its input range and also the output swing of the amplifier. By adjusting the value of the degeneration resistor $R$, the amount of feedback can be controlled so that an optimum gain can be achieved.

Figure 3 shows the simulated transfer curves of the amplifier with various values of degeneration resistor $R$. The gain of the amplifier without feedback ($A = 1$) is 20. The improvement of the gain is evident.

2.3. Differential Op Amp Design

Using the principle presented in Sections 2.1 and 2.2, we implemented a GaAs MESFET differential op amp. The op amp configuration is shown in figure 4. $T_1$ to $T_6$ make up the differential stage. $T_3$ and $T_4$ are active loads, and $T_5$ and $T_6$ are the tail current source. The voltage following inverting current mirrors \([^8\] $T_5$, $T_7$ and $T_4$, $T_8$ is used to provide inverted feedback signals to the active loads. $T_7$ and $T_9$ and level-shifting stage

$T_{11}$ and $T_{13}$ provide the positive feedback for the inverting output, and $T_8$, $T_{10}$, $T_{12}$, and $T_{14}$ make up the feedback network for the noninverting output. $R_e$ and $C_e$ are used for lead compensation. In this architecture, the inverted feedback signal for one of the active loads can be taken from the output of the other active load of the differential stage so that the "unity-gain inverter" shown in figure 2 is eliminated. The circuitry is thus simplified and the frequency performance is improved.

To obtain the desirable high gain, the gain stage must be biased at the edge of instability and the resultant loop gain must be as near unity as possible without exceeding it; i.e., the resultant output conductance must be made as small as possible and yet remain positive. As mentioned, the amount of feedback is controlled by the value of the degeneration resistor $R$. The process used to manufacture the op amp provides precision thin-film resistors, the value of which can be controlled as accurately as 0.1%. However, the device mismatches