Selective LPE-Growth of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ on Semi-Insulating InP

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Selective liquid phase epitaxy (SLPE) of high purity ($n = 2 \times 10^{15} \text{cm}^{-3}$) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ on SiO$_2$-masked (100)-InP:Fe substrates has been performed and investigated using Nomarski interference contrast microscopy and SEM. The infill growth was done at low temperatures (~585°C) directly into chemically (HCl:CH$_3$COOH:H$_2$O$_2$) etched cavities without melt-etching. Square and circular recesses of 2–3 μm depth and varying size (100–500 μm) have been used in contrast to common reported regrowth experiments in long channels. Enormously enhanced growth rates have been found within the small structures. Orientation dependent growth effects are described. The realization of selectively grown areas with flat surface morphology has been achieved which is important for optoelectronic integration.

Key words: LPE, Selective Epitaxy, InGaAs, InP, Structured Substrates, Optoelectronic Integration (OEIC)

INTRODUCTION

The monolithic integration of optoelectronic and electronic devices on semi-insulating InP substrates is of great interest in long wavelength optical fiber communication systems. On the receiver side integrated InGaAs PIN-FET combinations are considered to be very useful for reducing the stray capacitances as well as costs in comparison to hybrid receiver modules. In addition stability and reliability will be improved. In order to meet the different requirements of high performance pin-photodiodes and field-effect-transistors simultaneously within one single InGaAs/InP chip the conception of a planar embedded absorption zone for the photodiode$^{1,2}$ seems to be a promising approach. However the use of infinitely extended long channels for infill growth strongly restricts the design flexibility of the optoelectronic integrated circuits (OEIC's). Thus selectively grown limited small areas are more convenient to combine a planar embedded photodiode with FETs and other devices on the same chip.

In this work the LPE deposition of undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ into 100–500 μm recesses formed in semi-insulating InP substrates has been investigated.

Selective liquid phase epitaxy (SLPE) of binary III-V compounds has been reported by several authors some years ago for GaAs$^{3-7}$ Gap$^9$ and InP$^9$. From these studies the SLPE technique has turned out to be both a very promising and a very critical process. Appropriate growth conditions have to be worked out in detail for different materials and for the respective case of application. However, very few data concerning SLPE of InGaAs lattice-matched to InP are available up to now. LPE growth effects of InGaAs on structured InP have been reported by Chand et al.$^{10,11}$ They used unmasked InP wafers into which long channels were etched before growth. They observed poor nucleation on (111) sidewalls. Easier nucleation was found on (111)A than on (111)B faces. In contrast for the quaternary InGaAsP they detected easier nucleation on (111)B planes.$^{12}$ Similar results have been published for InGaAsP by Turley and Greene,$^{12}$ who used SiO$_2$-masked channelled substrates.

For small areas instead of long channels to be regrown the infill growth is expected to be more difficult, because both types of (111) planes are always present in principle. Therefore it is not possible to choose the easy orientations for regrowth only. Recently Chand and Houston$^{13}$ published some new results on localized LPE growth of InGaAs. They reported successful growth into circular recesses of 200 μm diameter which were in-situ melt etched through openings in spun-on silica film masks. In the present work we used CVD-SiO$_2$ masks and exclusively wet chemical etching for a more precise depth control of the cavities. A variety of different geometries for the recesses has been investigated. In order to achieve easy controllable growth rates low growth temperatures have been applied in this study.

Etching Studies

All investigations were performed on Fe-doped (100) InP semi-insulating substrates. These were first covered with 120–200 nm SiO$_2$ (silox process) and structured by standard photolithography techniques. In order to determine approximate growth conditions for selective epitaxy a special test pattern has been used (Fig.1a). Windows of square and circular shapes are formed in the SiO$_2$ having different sizes ranging from 100 to 500 μm. Therefore the influence of different orientations, geometries and dimensions during etching and growth experiments can be studied. The SiO$_2$-masked substrates

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were chemically etched by applying a solution of CH₃COOH:HCl:H₂O₂ (1:1:1), which is often denoted as KKI etchant. The etching resulted in 2–3 μm deep cavities. Figure 1b shows scanning electron microscope (SEM) perspectives clearly demonstrating the smoothness of the etched bottoms that can be achieved with the KKI etchant. Best results were obtained with an etchant cooled down to 12°C. Figure 2 shows our results for different etching times. Cleavage-planes perpendicular to the [011] and [011] directions, respectively, were investigated in an optical microscope as shown in Fig. 2a. A significant orientation dependency of the sidewall regions is evident. In the case of (011) cross-sections typical sidewalks consist of two different types of planes: vertical (011) and inclined (111)B faces. (011) cross-sections lying perpendicular to these, exhibit (111)A sidewall planes. These different crystal planes noticeably influence the following infill growth experiments. For a precise control of the etched depth of the recesses, the etching rate of the 12°C KKI solution used had to be determined. In Fig. 2b the etched depth vs etching time is plotted in a double logarithmic scale (full circles). For comparison the original KKI data for 20°C etching temperature have also been included (dashed line). The experimental results (full circles) are fitted very well by a straight line of slope one indicating an etch rate determined by surface kinetics. This allows for a better control of the etched depth.

**GROWTH CONDITIONS**

The epitaxy-process was carried out in an automated LPE system where the push mechanism as well as the temperature-time-cycles are computer controlled. A low temperature LPE process for deposition of high quality thin InGaAs layers on (100)-InP:Fe has been used, originally developed for the preparation of active regions in InGaAs-FET devices, so that this process can be easily applied to fabrication of pin-FET wafers. The epitaxial growth was initiated at about 585°C. The step-cooling method has been applied at supersaturations of 1°–5°C. The deposition was done directly into the chemically etched recesses without in-situ melt etching. The use of standard bakeout procedures resulted in high purity material with a background doping level of 2 × 10¹⁵ cm⁻³ (CV-measurements). These low doping levels have been achieved in spite of the SiO₂-preservation on the wafer during the growth process. They are one order of magnitude lower than those reported in previous studies.