A Study of Self-Aligned Formation of C54 Ti(Si$_{1-y}$Ge$_y$)$_2$ to p$^+$ and n$^+$ Si$_{0.7}$Ge$_{0.3}$ Alloys Using Rapid Thermal Annealing

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In this paper, solid state reactions of titanium with boron and phosphorus doped Si$_{0.7}$Ge$_{0.3}$ alloys have been investigated for application in a self-aligned germanosilicide process. Wet chemical etching of the germanosilicide with respect to unreacted Ti in a solution of 1:1:5 NH$_4$OH:H$_2$O$_2$:H$_2$O has been investigated. Characterization was performed using four-point probe sheet resistance measurements, x-ray diffraction, cross-sectional transmission electron microscopy, Nomarski optical imaging, and scanning electron microscopy. The C54 Ti(Si$_{1-y}$Ge$_y$)$_2$ phase was observed to form for reactions on both boron and phosphorus doped Si$_{0.7}$Ge$_{0.3}$ alloys. Grain structures of the C54 phases were found to be similar to grain structures of intrinsic alloy reactions with lateral grain dimensions on the order of 0.3 μm. Resistivities of 22 μΩ·cm have been determined for the boron and phosphorus reactions. Although the germanosilicide phases were observed to etch slowly in 1:1:5 NH$_4$OH:H$_2$O$_2$:H$_2$O, which is conventionally used in the self-aligned titanium silicide process, the much higher etch rate of titanium nitride compounds and unreacted Ti provided for a self-aligned germanosilicide process. A first anneal in a nitrogen ambient was found to be necessary to eliminate lateral silicidation over surrounding oxide during self-aligned germanosilicide formation.

Key words: Chemical vapor deposition (CVD), germanide, germanosilicide, LPCVD, rapid thermal annealing (RTA), RTCVD, self-aligned silicide, silicide, titanium

INTRODUCTION

The scaling of metal oxide semiconductor field effect transistors (MOSFETs) to smaller physical dimensions causes an increase in interconnect and parasitic series resistances of the devices. Silicides were initially used in microelectronic devices to lower the interconnect resistance at the gate level using a polycide (poly-Si plus silicide) stacked gate structure. As device scaling is continued, increases in parasitic source/drain series resistance, due to higher sheet resistances, limit the current drive capability of the devices. A self-aligned silicide process was then proposed, which enabled the simultaneous formation of silicide on the gate, source, and drain of the MOS-FET, thus reducing both the interconnect and series resistances. The first self-aligned silicide process was proposed by Shibata et. al. using Pt silicide. Self-aligned titanium and cobalt silicide processes quickly followed due to their lower resistivity and higher temperature thermal stability necessary for post silicidation processing in comparison to other silicides. Today, self-aligned titanium and cobalt silicides are commonplace and are used extensively in industry. However, a discrepancy still exists as to the better choice of silicide due to various electrical and process-related tradeoffs between these two silicides.

Recently, the use of Ge and Si$_{1-x}$Ge$_x$ alloys in conventional Si processing has gained interest for application in novel device structures relying on bandgap engineering. These structures include high emitter efficiency heterojunction bipolar transistors, high
mobility quantum-well channel MOS transistors\textsuperscript{15,16} and MOS gate electrodes for threshold voltage adjustment\textsuperscript{17,18}. Other applications of Si\textsubscript{1-x}Ge\textsubscript{x} alloys are based on the lower temperature processing capabilities of the material in comparison to Si for applications such as low thermal budget fabrication of thin film transistors.\textsuperscript{19,20}

Also, we have recently shown that Si\textsubscript{1-x}Ge\textsubscript{x} alloys can be deposited selectively on Si with respect to SiO\textsubscript{2} at temperatures as low as 600°C using rapid thermal chemical vapor deposition.\textsuperscript{21} Deposition rates at this temperature are on the order of 500Å/min., which provide a process that is compatible with single wafer manufacturing. A scanning electron micrograph (SEM) of selectively deposited Si\textsubscript{0.7}Ge\textsubscript{0.3} deposited onto exposed Si areas defined in a thermally grown SiO\textsubscript{2} layer is shown in Fig. 1. As observed in this figure, very smooth films with excellent deposition selectivity can be obtained. The selectively deposited Si\textsubscript{1-x}Ge\textsubscript{x} alloys have also been investigated as a solid diffusion source for forming ion-implantation-damage-free, ultra-shallow junctions in Si\textsuperscript{22} and as a sacrificial layer for consumption during silicidation for application in raised source/drain transistor technologies.\textsuperscript{23}

Many of the above-mentioned structures will require low resistivity contacts similar to those obtained from silicides. Therefore, an understanding of reactions between metals and Si\textsubscript{1-x}Ge\textsubscript{x} alloys is necessary. In order to implement titanium germanosilicide materials in the fabrication of these devices, processing issues concerning the reactions of Ti with doped Si\textsubscript{1-x}Ge\textsubscript{x} alloys and the effect of various wet chemicals on the germanosilicide need to be investigated. For some device applications, impurities may be incorporated into the Si\textsubscript{1-x}Ge\textsubscript{x} alloys to minimize the resistivity of the material as is done in Si. We have previously reported on the solid state reactions of Ti with intrinsic Si\textsubscript{1-x}Ge\textsubscript{x} alloys\textsuperscript{24,25} however, the incorporation of dopants in high concentrations may alter the reactions. Also, wet chemical etching is used in microelectronics fabrication in a variety of processes. These chemical etchants include NH\textsubscript{4}OH:H\textsubscript{2}O\textsubscript{2}:H\textsubscript{2}O, which is commonly used for cleaning or in the self-aligned silicide process. In this paper, we present results on the sheet resistance characteristics and minimum resistivity phase formation for solid state reactions of Ti with boron and phosphorus doped Si\textsubscript{0.7}Ge\textsubscript{0.3} alloys. Also, we have identified a self-aligned germanosilicide process for forming self-aligned contacts to Si\textsubscript{0.7}Ge\textsubscript{0.3} alloys.

Fig. 1. Selective Si\textsubscript{0.7}Ge\textsubscript{0.3} deposition on exposed Si defined in SiO\textsubscript{2} windows by rapid thermal chemical vapor deposition.

Fig. 2. Sheet resistance as a function of RTA temperature in both argon and nitrogen ambients for solid state reactions of Ti with (a) boron doped Si\textsubscript{0.7}Ge\textsubscript{0.3}, and (b) phosphorus doped Si\textsubscript{0.7}Ge\textsubscript{0.3}.\textsuperscript{26}