FLIP-CHIP REPLACEMENT WITHIN THE
CONSTRAINTS IMPOSED BY MULTILAYER CERAMIC
(MLC) MODULES

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(Received April 29, 1983)

ABSTRACT

Economics often dictates that suitable module
rework procedures be established to replace solder bump
devices (flip chips) reflowed to multichip carriers.
These operations are complicated, owing to various
constraints such as the substrate's physical and
mechanical properties, close proximity of surface
features, etc. This paper describes the constraints and
the methods to circumvent them. An order of preference
based upon the degree of constraint is recommended to
achieve device removal and subsequent site dress of the
residual solder left on the substrate. It has been
determined that rework (device replacement) can be
successfully achieved in even highly constricted
situations. This is illustrated by the example of
utilizing a localized heating technique, hot gas, to
remove solder from microsockets from which chips were
previously removed. Microsockets are areas to which chips
are reflowed to the top surface of IBM's densely populated
multilayer ceramic (MLC) modules, thus forming the
so-called controlled collapse chip connection or C-4. The
microsocket patterns are thus identical to the chip
footprint.
This paper also compares the physical and metallurgical joint characteristics of devices replaced by repair techniques with virgin-joined devices.

KEY WORDS: Multilayer ceramic, flip chips, controlled collapse chip connection, module rework, chip replacement, site solder dress, solder joint characteristics.

**Introduction**

Flip-chip bonding of devices has been routinely practiced by IBM for some time. All the chip I/Os, which are lead-tin solder pads, are joined to the substrate simultaneously by oven reflow forming the so-called controlled collapse chip interconnection (C4). Several methods have been practiced to prevent chip collapse due to solder run-off along the circuit pattern. Initially, screened-glass dams were utilized. More recently, this has been achieved through IBM's multilayer ceramic (MLC) packaging technology. Holes, called vias, are punched in the various ceramic layers while still in the green state. The pattern on the top surface exactly matches the chip's solder pads. Filled with metal, they constitute the method of vertical communication to the surface and provide the microsockets to which the chip is refloved (see Fig. 1). The solder volume is confined to the area of the microsockets, thereby preventing chip collapse.

A chip replacement capability is necessary for multichip carriers, such as IBM's 35, 50 and 90mm substrates, to accommodate manufacturing faults and engineering changes. Economic considerations preclude discarding populated substrates.

Typically, chip replacement consists of three separate processes: removal of a chip; dressing the residual solder left on the substrate; and repopulation of a chip at the replacement site.

Replacement operations must be performed and tools configured to overcome several package constraints while preserving the module's mechanical and functional integrity. This paper addresses these issues and details the metallurgy of joints after numerous device replacements.