We have investigated the effects of different annealing treatments on silicon dioxide films produced from the reaction of dichlorosilane and nitrous oxide at 700°C. The electrical quality of these LPCVD films was evaluated by measuring oxide charge and interface trap densities on metal oxide semiconductor (MOS) capacitors. These densities were measured before and after avalanche injection of electron currents into the oxide films. The results of these studies were as follows. (1) The LPCVD oxide films required a post deposition anneal at 1000°C to produce as-grown charge densities similar to those of a standard dry thermal oxide grown and annealed at 1000°C. (2) Post-injection charge densities of LPCVD films given a post deposition anneal at 1000°C were an order of magnitude greater than those of the standard dry thermal oxide. (3) Different annealing treatments produced a series of dominant electron trapping centers in the oxide bulk with capture cross sections ranging from $10^{-14}$ cm$^2$ to $10^{-17}$ cm$^2$. (4) The electron traps in the LPCVD oxides films were similar to those previously observed in standard wet thermal oxides grown and annealed above 1000°C.

Key words: oxide film, chemical vapor deposition, dichlorosilane, oxide charge, bulk traps, interface traps.
1 Introduction

Low fabrication temperatures provide the substrate dopant profile and defect control necessary for the full realization of VLSI (very large scale integration) within the silicon planar technology [1]. Therefore, low temperature processing sequences which optimize the electrical quality of silicon dioxide dielectric films are important in this technology. We have examined the electrical properties of 40 nm thick oxides films produced at 700°C by low pressure chemical vapor deposition (LPCVD). The time required to deposit such oxides was approximately two hours, which is orders of magnitude less than the impractical time required to grow thermal oxides of comparable thickness at comparable temperatures.

Specifically, we have investigated LPCVD oxide films fabricated from the gaseous reactions of both silane (SiH₄) and dichlorosilane (SiCl₂H₂) with N₂O [2]. The oxides formed from the silane/nitrous oxide reaction had non-uniform thickness and other undesirable characteristics. These were not investigated further. The oxide films formed from the dichlorosilane/nitrous oxide reaction exhibited the same physical characteristics as oxides deposited from this same reaction at 900°C. The 900°C deposition temperature is used to achieve high deposition rates (12 nm/min) appropriate to field and isolation dielectrics [3]. However, as was noted above, the 700°C deposition produced VLSI gate oxide thicknesses within a reasonable time.

We also studied the effects of both post-deposition annealing treatments (PDA) and post-metallization annealing treatments (PMA) on the electrical quality of dichlorosilane LPCVD oxides. The effects of similar annealing treatments for conventional high temperature (1000°C) dry thermal oxides were also investigated. In the context of the overall objectives of the present program, the thermal oxides, with post-oxidation anneal (POA) and PMA treatments, are standards for gate insulators. They were included in the present study specifically as a benchmark for our overall processing technology.

The electrical properties investigated were those