Thermomechanical Deformation of 1 μm Thick Cu-Polyimide Line Arrays Studied by Scanning Probe Microscopy

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Due to the lower dielectric constant than the currently used SiO₂ dielectric, several polyimides are being considered for use in multi-layer high density interconnects. However, the mismatch in out-of-plane coefficient of thermal expansion (CTE) between the Cu conductor and most spin-coated polyimides may cause interfacial failures. A scanning probe microscope was used to estimate the out-of-plane CTE for several 1 μm thick, spin-coated polyimides and to observe thermally induced deformation of Cu-polyimide test structures on Si. The change in relative height of arrays of parallel Cu and polyimide lines of various aspect ratios were imaged in air at room temperature and 97°C. Linear elastic, generalized plane strain finite element models for different out-of-plane CTEs were used to estimate the CTE from the profile changes. It was observed that narrow (≤1 μm) polyimide lines are more constrained from expansion than wider lines.

Key words: Atomic force microscope, coefficient of thermal expansion, interconnects, polyimide, thermal expansion

INTRODUCTION

The signal exchange rate of a computer chip with its peripherals is controlled by the wiring board. The speed of data transmission on the wiring board is determined by the dielectric constant of the insulator, the conductivity of the conductor, and the size of the features. Current high density interconnects (HDIC) are fabricated from aluminum conductors and SiO₂ dielectrics deposited on a silicon substrate. An alternate material system based on a Cu conductor and a polyimide dielectric is currently under development. The main advantage of using Cu instead of Al is its lower resistivity (1.7 μΩcm compared to 2.7 μΩcm). Polyimides have been fabricated with significantly lower dielectric constant than SiO₂ (2.3–3.5 compared to 3.9–4.1).1

The in-plane thermal properties of polyimides are well matched with those of the Si substrate which prevents the wafer from bowing during the fabrication process. One of the problems with this system, however, is the out-of-plane thermal expansion mismatch between the polyimide1,2 and the Cu. During the manufacturing process, the structure is heated to 350–400°C and the out-of-plane coefficient of thermal expansion (CTE) mismatch between the polyimide and the copper can cause sidewall decohesion and via deformation. Different polyimides have different out-of-plane coefficients of thermal expansion and those HDIC fabricated with lower CTE polyimides should have fewer failures due to thermal stress. Knowledge of the out-of-plane CTE is also required to estimate stresses using finite element models.1

This paper reports on the use of an atomic force microscope (AFM) to measure the out-of-plane expansion of different polyimides in HDIC. Because the polyimide film is so thin (1 μm), none of the existing methods have sufficient resolution to measure expan-
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1. Spin coat 1 μm thick polyimide layer at room temperature. Cure at 350°C.

2. Deposit 100 nm thick silicon nitride cap at elevated temperature.

3. Deposit and cure photoresist. Expose pattern.

4. Develop photoresist and ion etch unexposed polyimide. Remove exposed photoresist.

5. Deposit 30 - 40 nm thick Ta liner at elevated temperature.

6. Deposit Cu film

7. Chemo-mechanically polish to planarize Cu and polyimide.

8. Remove nitride cap by ion etching.

9. Repeat steps 1 - 8 to build multiple levels.

Fig. 1. HDIC manufacturing sequence.

The HDIC manufacturing process uses standard lithographic procedures and is shown in Fig. 1. First, a 1 μm thick polyimide layer in liquid form is spin-coated on a 0.5 mm thick silicon substrate. The polyimide is cured at 350°C in nitrogen. Second, a 100 nm thick silicon nitride cap is deposited on top of the polyimide at elevated temperature. Then the system is coated with photoresist and the pattern is exposed to UV light. Unexposed photoresist is removed by developer and the exposed silicon nitride and polyimide are etched out by reactive ion etching (RIE). After