Gallium arsenide digital integrated circuits

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Abstract. The motivations behind the development of GaAs integrated circuits (IC) are two-fold: to integrate high speed logic with optical sources and to meet the increasing demand of realising LSI/VLSI with higher speed and lower power dissipation for large scale computer applications. GaAs gigabit circuits have been growing in complexity to more than 3000 gates on a single chip. Although this is encouraging, more efforts are needed to improve production yield. By far the most work on GaAs digital IC has been done using MESFET as the active devices. MOSFET technology is yet to mature from the practical IC point of view. The logic-gate types used in circuits are predominantly of the enhancement-mode driver and depletion-mode load configuration (E/D).

A brief survey of the state-of-the-art of GaAs digital IC is presented. Implemented circuits are described and compared with those achieved through various technologies. GaAs gate arrays, multipliers, accumulators and memories are discussed. At liquid N₂ temperature, a switching time of 5.8 ps/gate has been achieved for 0.35 μm gate devices. This and similar other results lead to the conclusion that at the VLSI level of future Gbit circuits, GaAs devices in the form of HEMT operated at 77 K can outperform Si-devices. At LSI complexities, experimental GaAs MESFET and 300 K HEMT have a lead on Si-circuits—it is then this range in which Gbit/GaAs should find their application.

Keywords. GaAs digital integrated circuits; very large scale integration; heterojunction bipolar transistor; high electron mobility transistor; Schottky barrier gate.

1. Introduction

The present day integrated circuit (IC) industry is dominated by silicon, but the demand for high speed signal processing and large scale computer systems has focussed attention on alternative materials and devices. Among the 'non-silicon' materials, GaAs has been investigated quite extensively for realising high speed digital IC. Although laboratory test circuits fabricated on GaAs have shown much promise, commercial viability in terms of the level of integration, yield and design testability is yet to be established (Steger et al 1986).

Early enthusiastic claims that GaAs is potentially five to six times faster than silicon, is based on the ratio of the low field electron mobilities but this claim is unlikely to be valid in operational circuits (Bosch 1984). Investigations have revealed that the speed advantage of GaAs metal semiconductor field effect transistor (MESFET) over Si-bipolar and Si MESFET is between 2:1 and 3:1 for customised serial structure circuits. But this advantage will be largely lost in interconnect-intensive parallel structure configurations. The present state-of-the-art scarcely points to the possibility that GaAs will totally replace Si, but it will be wrong to underestimate the capabilities of GaAs-based materials which can be configured into a variety of hetero-structures with a wide range of exploitable physical phenomena. The switching performances of high electron mobility transistor(s) (HEMT) and heterojunction bipolar transistor(s) (HBT) appear to provide GaAs with a significant lead.

The aim of this paper is to place GaAs digital IC in proper perspective. Those
design approaches which are finding increasing applications in digital IC are discussed. Comparisons are made with typical logic family performances for different technologies on the basis of available data. Likely improvements in performance vis-a-vis applications in the near future are also summarised.

2. High speed applications–material choice

The realization of ultra-high speed very large scale integration (VLSI) necessitates achieving: (1) a very low gate propagation delay ($\tau_d$), (2) a low power per gate ($P_d$), (3) extremely low speed power product ($P_d \tau_d$), (4) very high gate densities, and (5) a very high yield. These in turn generate a number of requirements for the characteristics of the active devices needed to implement such circuits.

For a given power dissipation, the maximum allowable number of gates per chip or the maximum speed power product can be calculated for a given clock frequency, $f_c$ using the equation

$$P = 2Nf_c(P_d \tau_d) \ldots$$

(1)

where $N$ is the number of gates per chip.

The dynamic switching energies ($P_d \tau_d$) must exceed the stored energy on the switched capacitance $C$ (which is the sum of input capacitances of the fan-out of the loading gates plus the parasitic capacitance) i.e.

$$P_d \tau_d > \frac{1}{2}C(\Delta V_L)^2 \ldots$$

(2)

where $\Delta V_L$ is the logic voltage swing. More precisely the ($\Delta V_L$)$^2$ term is the product of $\Delta V_L$ and $V_{dd}$ (Eden 1980). Hence the logic swing voltage as well as the power supply voltage must be kept small for low values of $P_d \tau_d$. The requirement of small logic voltage swings dictates that the threshold voltages of the active devices involved should be very precisely controlled. In fact the standard deviation of the threshold voltages should preferably be less than 5% of the logic voltage swing (Eden 1980).

The current gain-bandwidth product of a field effect transistor (FET) in this near small threshold ($V_{gs} - V_T$) is given by

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{\mu_n}{2\pi L_g^2} (V_{gs} - V_T).$$

(3)

The propagation delay of a transistor with $N$ similar devices is given by

$$\tau_d = \frac{1}{\pi f_T} = \frac{2C_{gs}}{g_m}.$$

(4)

In order to have very low propagation delay, the devices must have high $g_m$ values which can be maximised by reducing the gate length. Dependence solely on the reduction of $L_g$ (i.e. placing unreasonable pressures on the required lithographic precision) will seriously affect the yield. Improvement can also be effected by using a semiconductor having higher channel mobility $\mu_n$. GaAs with about 6 times higher mobility than those for correspondingly doped bulk silicon is the natural choice for high speed FET devices. Very high electron channel mobilities of HEMT devices render a high value of $g_m$ and $f_T$ ideally suited for ultra-high speed digital circuits. The capacitance $C$ (eqn. 2) is to a large extent determined by the substrate capacitance of