ANALOG CIRCUIT IMPLEMENTATION OF NEURAL NETWORK WITH HIGH PRECISION WEIGHTS

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Abstract A current-mode MOS neuron circuit with 4-bit programmable weights is presented by using CMOS technology. The weights of the neuron have high resolution and also can easily be digitally stored. The resolution can be extended into high levels such as 8-bit, etc. by the design methodology presented in this paper. The operational principle of the neuron is discussed. Circuit simulation has been made by use of SPICE II. The results give a good agreement for the design requirements.

Key words Neural networks, Neurons, MOS integrated circuits

I. Introduction

The massive parallel processing and fault tolerant nature of artificial neural networks have attracted many researchers. The research concerning neural networks has focused mainly on theoretical studies and software simulation. However, simulations of neural network on Neumann serial computers are very slow, and future practical applications of neural networks depend strongly on hardware implementation. One of the main approaches of hardware implementation is electronic circuit realization. With the advance of VLSI technology, large neural networks can be integrated onto a single chip.

A current-mode neuron with 4-bit programmable weights using CMOS technology is proposed and discussed in this paper. The weights of this neuron have high resolution. Section II gives an analysis of the synapses of the proposed electronic neuron. The circuit for realizing the threshold function is described in Section III. Circuit simulation results are given in Section IV.

II. The Synapse Circuit

The synapse circuit for realizing the 4-bit programmable weights is shown in Fig.1. The weights $B_3, B_2, B_1, B_0$ are represented by the gate voltages of 8 MOS transistors $M_{S0}, M_{S10}, M_{S13}, M_{S14}, M_{S17}, M_{S18}, M_{S21}, M_{S22}$, where

$$B_i = \begin{cases} 0, & V_{D1} = -5V \\ 1, & V_{D1} = 5V \end{cases} \quad i = 0, 1, 2, 3$$

To implement the 4-bit weights, the width-to-length ratios of the 4 transistors $M_{S8}, M_{S12}, M_{S16}, M_{S20}$ and the other 4 transistors $M_{S7}, M_{S11}, M_{S15}, M_{S19}$ are respectively
as follows:

\[(W/L)_{MS_5} : (W/L)_{MS_{13}} : (W/L)_{MS_{11}} : (W/L)_{MS_{19}} = 8 : 4 : 2 : 1\]

\[(W/L)_{MS_7} : (W/L)_{MS_{11}} : (W/L)_{MS_{15}} : (W/L)_{MS_{19}} = 8 : 4 : 2 : 1\]

The bias of the circuit is formed by \(MC_1, MC_2, MC_3, MC_4\). With \(MC_3, MC_4\) as switch, the input voltage signal causes the currents in \(MS_1, MS_2\) to be either excitatory or inhibitory. When \(V_{in} = 5V\), the current received by \(MS_6\) will be excitatory \((I_+)_s\); and when \(V_{in} = -5V\), the current received by \(MS_5\) will be inhibitory \((I_-)_s\). For each synapse, the output current of the neuron is

\[
I = (2^3 \cdot B_3 + 2^2 \cdot B_2 + 2^1 \cdot B_1 + 2^0 \cdot B_0) \times I_{min} \times f(V_{in})
\]

where \(I_{min}\) is the minimum value of the excitatory current \((I_{+min})\) or the inhibitory current \((I_{-min})\), determined by \(M_{20}, M_{10}\) respectively. Also

\[
I_{min} = I_{+min} = I_{-min}
\]

\[
f(V_{in}) = \begin{cases} 
1, & V_{in} = 5V \\
-1, & V_{in} = -5V 
\end{cases}
\]

It follows that the circuit designed in Fig.1 performs the multiplying operation of the input voltage and the weights. The summing of the excitatory currents and inhibitory cur-