A Maximum Time Difference Pipelined Arithmetic Unit Based on CMOS Gate Array

Tang Zhimin (唐志敏)¹ and Xia Peisu (夏培肃)
Institute of Computing Technology, The Chinese Academy of Sciences, Beijing 100080
Received June 6, 1994.

Abstract

This paper describes a maximum time difference pipelined arithmetic chip, the 36-bit adder and subtractor based on 1.5 \( \mu \)m CMOS gate array. The chip can operate at 60MHz, and consumes less than 0.5Watt. The results are also studied, and a more precise model of delay time difference is proposed.

Keywords: Adder, CMOS, gate array, maximum time difference, wave pipeline.

1 Introduction

Maximum time difference pipelining, also called wave pipelining, is an effective approach to promote the clock frequency of computing engine. Different from conventional pipeline technique, the increase of clock frequency in maximum time difference pipelined devices does not rely on the insertion of interior storage elements (latches, flip-flops, etc.) into the circuit, hence the total latency of the circuit is not changed.

In 1986, we built an experimental maximum time difference pipelined processor using ECL SSI and MSI chips with gate delay of 2.0ns and attained a clock period of 9.8ns (102MHz)[4]. The multiplier of the processor was constructed with devices with 0.8ns gate delay, and its minimum cycle time was 5.5ns.

This paper introduces our recently completed LSI arithmetic chip with maximum time difference pipelining technique. Although 1.5\( \mu \)m CMOS gate array is a kind of slow process, our chip can work at clock frequency of 60MHz. The chip has TTL compatible electric interface and dissipates less than 0.5Watt.

2 Logic Design of the Adder

2.1 Pipelined Carry Look-Ahead Adder

Considering that design period is limited and the basic cells are only normal CMOS gates and flip-flops, the carry look-ahead (CLA) scheme is applied to design

¹E-mail: tang@chpc.ict.ac.cn
Project supported by National Natural Science Foundation of China under grant No.9689009.
our 36-bit adder.

To decrease the number of transistors used, traditional CLA adders use the structure as shown in Fig.1, where the carries generated in CLA unit is feed back into group adders. Such a structure can add at most one pair of operands within the total delay of the adder, i.e., the clock period cannot be less than the latency of the adder.

![Fig.1. Conventional 16-bit carry look-ahead adder.](image)

To increase the clock frequency of an adder, the adder itself can be pipelined. Thus the feedback in Fig.1 should be cut off. The corresponding adder structure is shown in Fig.2, where GP units are used only for producing generation and propagation signals, and the sum is formed in F units.

![Fig.2. Pipelinable 16-bit carry look-ahead adder.](image)

2.2 Grouping Considerations of the 36-bit Adder

Grouping is essential to implement engineering feasible CLA adders. For 36-bit adder, there are several possible grouping schemes, such as $6 \times 6$, $4 \times 4 \times 3$, $3 \times 4 \times 3$, $3 \times 3 \times 4$. To select which scheme, not only logic stages, but also fan-in and fan-out of all macro and basic cells and their impacts on transmission delay must be analyzed. For example, the $6 \times 6$ scheme is a kind of one-level grouping, just like that shown in Fig.1 and Fig.2, so the number of logic gate layers is the least among