CMOS LED-driver and PIN-receiver for fiber optical communication at 155 Mbit/s

Jan SEVENHANS *
Wim DELBARE *
Michel STEYAERT **
Mark INGELS **
Jan VANDEWEGE ***

Abstract

A test chip for an integrated full CMOS LED driver has been realized with a modulation current of 60 mA at a maximum bit rate of 155 Mbit/s. A CMOS receiver is evaluated to amplify PIN diode photo currents less than 10 μA at the same bit rate of 155 Mbit/s. Both circuits are integrated on one chip. The circuit has been developed in a 0.8 μm digital CMOS process.

Key words: Integrated circuit, Complementary MOS technology, Optical transmitter, Optical receiver, Control circuit, Interface circuit, Interconnection, Wide band circuit.

Contents

I. Introduction.
II. Background: application of optical interconnections in broadband digital exchanges.
III. Receiver.
IV. Driver.
V. Measurements.
VI. Conclusion.
References (5 ref.).

I. INTRODUCTION

To achieve high reliability and cost-effectiveness in short distance optical fibre communication systems the application of single chip CMOS integrated circuits is indispensable [1]. The objective of this work is to integrate the receiver, the digital signal processing and the driver on one CMOS chip, with as low as possible extra external components. For the application at 155 MHz clock rate we choose to use LEDs instead of lasers. In this contribution both a high speed CMOS receiver and transmitter are presented. They are designed in a standard 0.8 μm digital CMOS process to ensure compatibility with existing digital signal processing circuits. The receiver/driver has been designed to use commercially available PIN-diodes and LEDs.

* Alcatel Bell Telephone Francis Wellesplein 1, B-2018 Antwerp, Belgium.
** Catholic University of Leuven Kardinaal Mercierlaan 94, B-3030 Leuven, Belgium.
*** University of Gent Sint Pieters Nieuwstraat 41, B-9000 Gent, Belgium.

Ann. Télécommun., 48, n° 3-4, 1993
II. BACKGROUND: APPLICATION OF OPTICAL INTERCONNECTIONS IN BROADBAND DIGITAL EXCHANGES

The physical realisation of broadband digital exchanges imposes very hard requirements on interconnection and packaging technologies. Three problems come together: high speed interconnections (150 or 600 Mbit/s, requiring impedance controlled paths), high density, and high thermal dissipation. Interconnection distances vary between 10 cm (shortest interconnection between 2 chips in the same subrack, via backpanel) and 100 m (longest interconnection between two chips in different racks, via cable). It is the simultaneous existence of the three requirements which is cause of important problems. For example, high density implies the need for fine line printed circuit boards and backpanels. Controlled impedance implies accurate control of trace widths. Obtaining narrow tolerances on fine lines requires application of the most advanced circuit board processing technologies.

To overcome the limitations of electrical interconnection systems, an optical interconnection technology based on the combination of multimode optical fibers and discrete wiring is being developed [4, 5]. The discrete wiring technology allows embedding of copper wires and glass optical fibers in multilayer laminate substrates, to obtain electro-optical circuit boards and backpanels. Via surface optical taps and short fiber pigtails contained inside multifiber packages, light is coupled in and out of the embedded fibers. Fiber ribbon cable and a board to ribbon cable connector complete the optical part of the interconnect system to form a solution for high speed optical interconnections over the whole range of distances required in broadband exchanges. The technology of discrete wiring boards with surface optical taps, the multifiber packaging, the board to ribbon cable connector are currently under investigation in the Race 2048 HIBITS project. The multimode fiber interconnections can be used with LEDs or lasers. In this paper, CMOS driver and receiver circuitry for an LED based interconnection is discussed.

Realisation of driver and receiver circuits in CMOS should lead to the possibility of monolithic integration of optical driver and receiver circuits with the complex digital functions required in broadband exchanges. The LED and photodiode are then the only extra chips required to replace electrical interconnections by optical interconnections.

Over distances below hundred meter, the optical losses of the graded index multimode fibers are negligible. In the path, however, there are several fiber to fiber connections: between the multifiber package and the board, at receiver as well as at transmitter side, and between board and cable or between board and backpanel, again at receiver and at transmitter side, resulting in a typical number of 4 fiber to fiber connections in the optical path. The fiber to fiber connections are being designed in Race HIBITS for a worst case loss of 1 dB. The fiber to fiber connections will be determining for the optical power budget. With an expected 20 μW of optical power launched into the multimode fiber from an LED driven at 60 mA current, and 4 fiber to fiber connections in the path, an optical power of about 8 μW can be expected on the detector. With a detector responsivity of 0.5 A/W, currents in the order of 4 μA have to be detected.

For these power budget specifications, a CMOS based LED-driver/PIN diode receiver pair was designed, to operate at a serial speed of 150 Mbit/s.

III. RECEIVER

The receiver detects the photo current and converts it to an electrical signal. The optical part consists of a PIN-diode. In Table I the characteristics of a usable diode for this purpose are presented. The diode converts light into a current. It can be assumed that the modulation current is ± 5 μA. The receiver has been designed to detect currents up to ± 15 μA. Larger currents cause saturation. The minimal current is limited by transistor mismatching and noise.

<table>
<thead>
<tr>
<th>Type</th>
<th>MSP 1E 200 PIN diode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Responsivity</td>
<td>0.5 A/W</td>
</tr>
<tr>
<td>Rise time</td>
<td>1 ns (5 V)</td>
</tr>
<tr>
<td>Fall time</td>
<td>1 ns (5 V)</td>
</tr>
<tr>
<td>Capacitance</td>
<td>0.2 pF</td>
</tr>
</tbody>
</table>

The receiver (Fig. 1) is a three-stage transconductor, followed by a string of inverters. The basic function of the amplifier sections is a current → voltage → current conversion (Fig. 2). The transfer function of this circuit is:

\[ i_{out} = g_m R_{pin}. \]

An interesting feature of this circuit is that in absence of photocurrent the dc levels of node 1 and node 2 are equal, if both the transistors \((M_1 & M_2)\) and the current sources \((I_1 & I_2)\) are the same. By this, the amplification sections can easily be put in series, without any difficulty concerning the biasing. From simulations on the circuit of Figure 2, stability problems in the current to voltage part were detected. To examine this effect the small signal circuit diagram of the circuit (Fig. 3) has been analyzed. The transfer function is:

\[ i_{out} = g_m R_{pin}. \]