ON THE SYSTEM AND ENGINEERING DESIGN OF THE GENERAL PURPOSE ELECTRONIC DIGITAL COMPUTER AT T.I.F.R.

BY R. NARASIMHAN

(Tata Institute of Fundamental Research, Bombay)

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1. INTRODUCTION

Since 1955, the Computer Section of the Tata Institute of Fundamental Research has been engaged in the development and construction of a large-scale electronic digital computer for doing scientific computations. As a preliminary to this, a pilot digital calculator was designed and completed in September 1956 and was kept in operation for about a year. The design of the full-scale machine was started early in 1957 and its final assembly completed in February 1959. Unfortunately, owing to the lack of air-conditioning facilities, the work had to be suspended till almost the end of 1959. The actual testing was begun in mid-November 1959 with an auxiliary air-conditioning system and the computer was commissioned for routine work in the third week of February 1960. This paper describes briefly the main features of the system and engineering design of this digital computer. In a companion paper, some aspects of the circuitry will be dealt with.

The T.I.F.R. computer is a parallel, binary, asynchronous machine. It is controlled by a stored programme of single-address instructions and has a fast access ferrite-core memory consisting of 1,024 locations. The input to the computer is by means of a punched paper tape (5-hole commercial teletype tape) and the output can be either printed out directly or punched on a paper tape again.

Both in the system and engineering design, the principal emphasis has been on reliability of operation and ease in maintenance. With this in view, the logical circuit types have been kept to the minimum consistent with flexibility and the wired circuits were put through a rigid acceptance test to check their performance under extreme operating conditions. For rapid fault localization and servicing, a large part of the computer has been assembled
in terms of functionally self-contained packaged units. Separate testing facilities have been set up for routine checking of these plug-in units.

The main computer assembly has 2,700 tubes (almost all of them double-triodes), 1,700 crystal diodes (germanium) and approximately 12,500 resistors. Since the computer is d.c. coupled throughout, few condensers are used and except in the case of two bias supplies, no circuit is transistorised. The total power consumption is about 18 K.W.

2. The Arithmetic and Control Logic

In the T.I.F.R. computer, all the internal operations take place in the binary notation and numbers are stored in the main memory as signed binary fractions restricted to the range \((-1, 1\) ). A number in its normal form consists of a sign (which is a 0 for positive numbers and a 1 for negative numbers) followed by 39 binary digits (bits, for short) which give its absolute value as a binary fraction. The binary point is understood to be fixed immediately after the sign bit (see Text-Fig. 1). The complement form of a number is obtained by changing all its 1’s to 0’s and vice-versa; the sign bit is left unaltered, however, in this process.

A schematic diagram of the arithmetic unit is shown in Text-Fig. 2. It consists of an adder, a memory register and two (double rank) shift registers (the accumulator and MQ-register, respectively) and a pair of true/complement gates. The adder is of the fast logical type and incorporates in itself special carry by-pass facilities to speed up the carry propagation time. These cut down the addition time to about one-third of what it would otherwise have been. The contents of the accumulator are presented to the adder either in the true or the complement form depending on whether the operation called for is addition (multiplication) or subtraction (division) respectively. In some cases the result of a subtraction needs to be recomplemented to obtain the number in its true form. To simplify this procedure, facilities have been built into the adder so that its output can be gated into the accumulator either in its true or complement form. Also the particular design of the adder used makes it especially simple to obtain the logical product of the adder inputs and this is taken advantage of in the Collate order.