Power consumption reduction in Systems on Chip (SoCs)

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Abstract

Systems on Chip are becoming extremely complex integrated circuits, containing tens or hundreds of analog, RF and digital blocks. For most applications, they have to present extremely low power consumption. It is the case, for instance, in ad hoc networks for which 100 or 1000 SoC nodes have to sense their environment, do some processing and send by radio some information to adjacent nodes in a multi-hop fashion to reach finally a base station. The design of such SoC nodes, to achieve the required extremely low power consumption, has to be performed first at the system level, including low power communication protocols and data routing through the network, node wake-up strategies, low-power software and operating systems, innovative solutions for the sensor part, flexible or reconfigurable and very low power digital processing, low-power networks on chip for the communication between embedded processors and memories, as well as low power RF front-ends. In addition, due to the impressive technology pace, new problems have to be solved for the design of SoCs, such as the interconnect delays, reliability and the dramatic increase of the static power. Some techniques, considered as the most efficient, of dynamic as well as static power reduction are described. It is however shown that the design of SoCs in 130 nm and below will impact dramatically the design methodologies, mainly due to the static power increase. Finally, if today most SoCs are powered by batteries, alternative sources of energy are reviewed.

Key words: System on chip, Energy consumption, Electric power, Mobile radiocommunication, Ad hoc network, Low energy, Electric source.

RéDUCTION DE LA CONSOMMATION DE PUISSANCE DANS LES SYSTÈMES SUR PUCES

Résumé

Les Systèmes sur Puce deviennent des circuits intégrés extrêmement complexes, contenant des dizaines ou des centaines de blocs analogiques, radio et numériques. Pour la majorité des applications, ils doivent présenter une consommation de puissance électrique extrêmement faible. C’est le cas, par exemple, des réseaux d’objets communicants, dans lesquels une centaine ou un millier d’objets doivent sonder leur environnement, effectuer un traitement numérique et envoyer par radio des informations à des objets voisins en plusieurs sauts vers une station de base. La conception des ces systèmes sur puce, pour parvenir à des consommations très basses, doit se faire premièrement au niveau système, considérant des

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It is predicted that transistor dimensions will shrink below 30 nm in the next few years, while the number of devices on a typical chip will soon reach one billion and above. Such a complexity, achieved through innovations in device design and fabrication technologies, leading to Systems on Chips (SoCs), needs to be matched by fundamentally new design approaches and methodologies. In the near future, concepts such as embedded high-performance computing systems, reconfigurable computing, and ultra-low-power operation will become essential features of these highly integrated systems. At the same time, communication applications - and especially, wireless communication - are emerging as the dominant domain of implementation for very high performance digital integrated systems. Numerous aspects of distributed wireless communication networks will also need to be investigated to fully exploit the possibilities of their utilization in the context of distributed computing, network-wide energy management, dynamic reconfigurability, and intelligent resource allocation.