EMBEDDING RECTANGULAR GRIDS INTO SQUARE GRIDS

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Abstract. We show that 2-dimensional rectangular grids of large aspect ratio can be embedded into rectangles of smaller aspect ratios with small expansion and dilation. In particular, width can be reduced by a factor of up to 2 with optimal expansion and dilation (2). A factor of 3 can be obtained with dilation 3. In general, any rectangular grid can be embedded into a square grid that is no more than unity larger on the side than the minimum possible, with dilation no more than 3. These results improve on those previously obtained, in which dilation better than 18 could not be guaranteed. They might be applied to more complex grid embedding problems, such as embedding multi-dimensional grids into hyper-cubes.

1. Introduction

An embedding of a guest graph \( G = (V_G, E_G) \) into a host graph \( H = (V_H, E_H) \) is a one-to-one mapping \( \phi \) from \( V_G \) to \( V_H \). We measure the quality of an embedding \( \phi \) with two cost functions: dilation and expansion. The dilation of an edge \( \{u, v\} \in E_G \) is the length of a shortest path in \( H \) that connects \( \phi(u) \) and \( \phi(v) \). The dilation of an embedding is the maximum dilation, over all edges in \( E_G \). The expansion of an embedding is \(|V_H| / |V_G|\). The dilation of an embedding measures the worst case stretching of an edge, the expansion measures the relative size of the guest graph. One can also define a load factor, which measures the worst case sharing of an edge in the host by paths from the guest. We do not consider load factors in this paper, except to note that, in the embeddings under consideration, it is small.

Embedding problems can model many questions of interest in Computer Science, such as VLSI circuit layout, simulating one parallel processing architecture by another, assigning processes to processors in a distributed processing system and simulating one data structure by another. Aleliunas and Rosenberg [1] considered the particular problem of embedding 2-dimensional rectangular grids of aspect ratio greater than one into smallest possible grids of square aspect. They point out that the problem has application to the design of large scale integrated circuits since the natural design of a circuit may be rectangular but the circuit must eventually be manufactured on a square chip. The critical factors of area and wire length are represented by expansion and dilation in the model just described.

A solution to this two dimensional problem may be used to solve more complex problems. For example, Bettayeb, Miller and Sudborough [2] discuss the embedding of multi-dimensional grids into hypercubes, which has immediate application to the efficient simulation of grid-like parallel processing architectures by hypercube architectures.

Aleliunas and Rosenberg were unable, in general, to optimise both expansion and dilation simultaneously and conjectured that there may be an inherent expansion-dilation tradeoff. If expansion is minimized, i.e., we embed a rectangular grid into the smallest possible square grid, then the smallest dilation they obtain depends on the aspect ratio of the rectangle. For some aspect ratios, dilation is optimal, i.e., 2, but for others dilation better than 18 could not be guaranteed.

In Section 2 we summarise the results obtained in this paper. In Section 3 we describe an improved compression technique suitable for instances of the problem with smaller aspect ratios. In Section 4 we show that the new compression technique can be combined with an earlier technique called "folding" to obtain a close to optimal result for any aspect ratio.
2. Summary of New Results

Our results show that there is in fact no significant tradeoff between expansion and dilation, for this problem. In many cases optimal expansion and optimal dilation can be achieved simultaneously and in the worst case dilation 3 is obtainable with almost optimal expansion.

Let the rectangular grid be of height $h$ and width $w$ and let $h < w$. Let $h' < h$ and $w'$ be the smallest integer such that $h'w' \geq hw$. We call the $h' \times w'$ rectangle the *ideal rectangle* and the ratio $w/w'$ the *compression ratio*. We will call the square grid of side $s$ where $s = \lceil (hw)^{0.5} \rceil$ the *ideal square grid* and the square of side $s+1$ the *nearly ideal square grid*. The following theorems will be proved.

**Theorem 1:** If the compression ratio is $\leq 2$, then a rectangular grid can be embedded into any of its ideal rectangular grids with dilation 2.

**Corollary 1:** If the compression ratio is $\leq 2$, then a rectangular grid can be embedded into its ideal square grid with dilation 2.

**Theorem 2:** If the compression ratio is $\leq 3$, then a rectangular grid can be embedded into any of its ideal rectangular grids with dilation $\leq 3$.

**Corollary 2:** If the compression ratio is $\leq 3$, then a rectangular grid can be embedded into its ideal rectangular grid with dilation $\leq 3$.

**Theorem 3:** Any rectangular grid can be embedded into its nearly ideal square grid with dilation $\leq 3$.

3. Small Compression Ratios

In this section we justify Theorems 1 and 2 and hence their corollaries. We will consider compression ratios up to 3 in this section, but we illustrate the general technique in terms of the smallest of these, i.e., in the range 1 through $3/2$. Other cases are then covered by generalising at the end of the section.

3.1. Primitive Tiles

We first define a simple compression pattern that embeds any $(n-1) \times n$ grid into a $n \times (n-1)$ grid. This pattern, which for a particular $n$ we call a primitive, light 2-tile, is defined in Figure 3.1.a The tile shown there represents an embedding of a $4 \times 5$ grid into a $5 \times 4$. The figure shows the position of the edges that were horizontal in the guest grid, after the embedding into the host. A diagonal edge indicates that adjacent nodes have been embedded across the diagonal of a unit square in the host. There are two shortest paths between the images of these nodes, of length 2. The vertical edges are not shown but their position is easily deduced. We note that the dilation of no edge, vertical or horizontal, is greater than two. Note that the pattern can be extended *ad infinitum*.

![Figure 3.1 Light 2-Tiles](image-url)