Interface trap density in amorphous La$_2$Hf$_2$O$_7$/SiO$_2$ high-$\kappa$ gate stacks on Si

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ABSTRACT The present paper investigates the interface trap density of a new high-$\kappa$ gate dielectric stack, La$_2$Hf$_2$O$_7$/SiO$_2$ on Silicon. Amorphous La$_2$Hf$_2$O$_7$ thin films are deposited by metal evaporation in the presence of atomic oxygen beams on an ultra-thin SiO$_2$ layer (1.5 nm) grown by rapid thermal oxidation on a $p$-type Si substrate. A combination of electrical (C–V) and cross sectional TEM measurements indicates a value of the dielectric constant $\kappa$ of about 19 ± 2.2. The interface state density ($D_{it}$) was measured using the conductance method for different La$_2$Hf$_2$O$_7$ thicknesses ranging from 3 nm to 14 nm. $D_{it}$ ranges from $3.4 \times 10^{10}$ eV$^{-1}$ cm$^{-2}$ to $4.8 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$ and shows a quasi-linear dependence on the La$_2$Hf$_2$O$_7$ layer thickness. The interface state density increase with film thickness could have different explanations, such as oxygen de-passivation and/or defect generation at the Si-SiO$_2$ interface, formation of a new Si-SiO$_2$ interface by Si oxidation or alternatively, the SiO$_2$ interfacial layer reduction by oxygen vacancies.

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1 Introduction

In recent years the down scaling of MOSFET devices has revealed the physical limit of silicon dioxide as gate dielectric. Basically, there are two limitations in using SiO$_2$ as gate dielectric in CMOS technology. First, for ultra-thin SiO$_2$ films under 7–8Å the structure is distorted and the bulk structural properties such as energy band-gap and band-offsets with silicon are drastically affected [1, 2]. This prevents proper functioning of any MOSFET based on SiO$_2$. Second, for gate oxides as thin as 13–15 Å, the gain of MOSFET can be achieved only at the expense of relatively large power consumption and these devices are not usable for low power applications. This is due to high leakage current densities of 1–10 A/cm$^2$ originating from direct tunnelling currents at relatively low gate biases [2–4]. The tunnelling and the associated effects cannot be avoided in the present configuration and one solution could be to replace the silicon dioxide as gate dielectric with a high-$\kappa$ oxide. In this way the physical thickness of the gate dielectric is maintained in a range where the tunnelling currents are negligible while the specific capacitance could continue to increase. The search for new gate dielectrics has initially encompassed a wide range of materials such as Ta$_2$O$_5$ [5, 6], Al$_2$O$_3$ [7, 8], Y$_2$O$_3$ [9–11], HfO$_2$ [12–14], ZrO$_2$ [15–17], La$_2$O$_3$ [11] whereas ternary compounds are rarely investigated. A notable exception is SrTiO$_3$ [18–20], but this is of interest mostly as a model system due to the rather low conduction band offset with Si [21–23]. The alternative gate dielectric should fulfill some requirements in order to integrate into the CMOS technology. Reactions with Si at temperatures as high as 900 °C are not desired in order to preserve high effective dielectric constant for the gate dielectric stack, which otherwise would be increased by the interface layer formed by reactions’ products [24, 25]. As a second major constraint, the band offsets of the new oxide with Si and gate electrode should be at least 1 eV for an effective reduction of the leakage currents [26]. Presently, most of these oxides do not possess the desired properties needed for gate applications.

In this paper we investigate one of the potential candidates for high-$\kappa$ gate applications, La$_2$Hf$_2$O$_7$ (LHO), which belongs to the ternary oxides class. This is a cubic material with space group symmetry $Fd3m$ [27], which is very similar to silicon. Also, the lattice constant of LHO is about two times that of silicon and presents a lattice mismatch of $\sim 0.74\%$ at room temperature and effectively zero at around 800 °C. Therefore, it is well suited for epitaxial growth on Si (001). In addition, the La$^{3+}$ ion possesses a large polarizability of 6.07 Å$^3$ [28], so that the electronic contribution to the dielectric constant is expected to be high. Amorphous LHO, such as the one studied in this paper, could be a good candidate because there is an evidence that the introduction of La in HfO$_2$ increases the crystallization temperature above 950 °C [29].

One of the key requirements for high-$\kappa$ gate oxide films is a low trap density $D_{it}$ at the interface with silicon in order to fit the operational MOSFET parameters. For many decades the SiO$_2$-Si system, which is obtained simply by oxidizing the silicon substrate, has represented a remarkable system with a very low interface trap density in the order of $10^9$ eV$^{-1}$ cm$^{-2}$. The continuous improvement of SiO$_2$-Si interface properties has been possible due to two unique features of this interface. First, it is a quite abrupt interface and the dangling bonds at the Si surface are suppressed either by pairing of Si–Si bonds or by placing bridging oxygen dangling bonds...
on the SiO₂ side between the pairs [26] as a consequence of the very large flexibility of the SiO₂ network. Second, injection of hydrogen atoms with a high diffusion rate by means of a simple forming gas anneal (FGA) further removes states in the gap. This excellent behaviour of the SiO₂-Si interface seems to be unique and hard to replicate in any high-κ oxide-Si interface obtained by direct deposition of the high-κ oxide on silicon. An alternative to the direct deposition on Si is the controlled insertion of a thin SiO₂ interfacial layer which could preserve the SiO₂-Si interface properties, in expense of a larger equivalent oxide thickness (EOT) value. In this paper we study the interface properties of the La₂Hf₂O₇/SiO₂/Si system as a function of the thickness of the high-κ oxide.

The properties of La₂Hf₂O₇ thin films deposited on Si or SiO₂ were not reported so far and the expected high dielectric constant could make it a good candidate for high-κ gate dielectric applications.

2 Experimental

The LHO films were prepared by molecular beam epitaxy (MBE), in a DCA 600 system. Prior to deposition an ultra-thin (15 Å) SiO₂ layer had been grown by rapid thermal oxidation (RTO). P-type Si(001) substrates (ρ ≈ 2–5 Ω cm) were used. After one hour pre-deposition anneal at 200°C under 2 × 10⁻⁶ Torr oxygen pressure, the substrates were brought to the deposition temperature of 550°C. LHO layers were deposited by coevaporating Hf and La metals in the presence of atomic oxygen beam. This beam was produced by a plasma source of Oxford Applied Research operating at RF power of 350 Watt with O₂ flow equivalent to a partial pressure of 4 × 10⁻⁶ Torr in the chamber. Hf was evaporated from an e-beam source at a rate of 0.18 Å/sec, while La was evaporated using a high temperature effusion cell with Ta crucible at 1720°C to produce a rate of 0.3 Å/sec. These rates were chosen so as to produce the stoichiometric composition La: Hf = 1:1, which was verified by energy dispersive X-ray analysis in scanning and transmission electron microscope. The thicknesses of the LHO films were 3, 7, 11 and 14 nm. To check structure and thickness of the layers high resolution transmission electron microscopy investigations of cross section samples were performed at a JEM-4010 microscope at 400 kV. Before metallization all samples received a forming gas anneal (10% H₂ + 90% N₂) at 420°C for 30 min. Gate contacts were defined by deposition of a 50 nm thick Mo layer on the LHO film followed by lithography and wet etching using a dilute basic oxidizing solution, consisting of Ammonia/Hydrogen Peroxide/Water (1 : 1 : 4). 100 nm thick Al was evaporated as a backside electrode. Capacitance and conductance measurements were performed using the HP 4194A and HP 4192A impedance analyzers. The interface trap density was evaluated using the conductance method developed by Nicollian and Goetzberger [30, 31].

3 Results and discussions

High frequency capacitance in a parallel capacitance-conductance equivalent circuit and phase angle difference of AC gate current and voltage were initially measured in order to determine the flat-band voltage, EOT, and dielectric constant of the oxide stack. In Fig. 1, the electrical characteristics of a sample with nominal physical thickness of 7 nm are shown. We observed that for the first C-V measurement a strong inversion layer at Si surface is established indicating a large amount of positive charge in the oxide. After performing a short negative gate bias stress, the C-V characteristics change into normal and stable ones. This behaviour is probably related to the high density of oxygen vacancies in the oxide film, which can be collected at room temperature under a suitable electric stress near the oxide-gate interface. Part of the flat band voltage shift is due to the workfunction difference (Φ_m ≈ −0.4 eV) between the Mo gate and the p-type substrate, while the rest is attributed to the presence of a positive fixed oxide charge. The work functions for Mo and p-type Si are considered 4.6 eV [32] and 4.99 eV, respectively. In the depletion region the decrease of the phase angle originates from the interface state conductance peak, whereas in the accumulation and inversion regimes phase angle values of about 90° indicate a small leakage current influence on the respective accumulation and inversion capacitances (Fig. 1). We consider that the MOS gate oxide stack capacitor consists of a combination of the high-κ oxide layer capacitance and the capacitance of the SiO₂ interfacial layer connected in series. The total capacitance was approximated by the capacitance measured in accumulation without quantum corrections.

To obtain the dielectric constant of the LHO film transmission electron microscopy (TEM) analysis was performed on the 7 nm thick sample. The TEM image (Fig. 2) shows amorphous LHO and SiO₂ layers on (001) Si as well as a good quality of both Si/SiO₂ and SiO₂/La₂Hf₂O₇ interfaces. The thickness of SiO₂ and La₂Hf₂O₇ layers determined from the TEM images are 15.7 Å and 57 Å, respectively. The thickness of the SiO₂ interfacial layer is close to the initial RTO layer thickness (15 Å), while the LHO layer is thinner than the nominal thickness of 7 nm. Considering the physical thicknesses of the LHO layer and of the interfacial layer for this sample and the gate oxide stack capacitance from Fig. 1, the dielectric constant of the LHO layer is estimated to be about 19 (+/− 2.2).

Evaluation of the interface density of states (Dₛ) and the time constant for different gate voltages in the depletion