High aspect ratio micromachining (HARM) technologies for microinertial devices

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Abstract In this paper, we review work on novel, high aspect processes for microinertial components at the Defence Evaluation and Research Agency (DERA). High aspect components may lead to significant cost-performance improvements in both accelerometers and gyroscopes. We have evaluated 3 low temperature process technologies – silicon on insulator (SOI) HARM, UV electroforming and bulk HARM. Prototype microinertial devices fabricated in these technologies are also presented. The potential of the processes for integration with on-chip CMOS electronics is assessed which may be either as part of a fully integrated MEMS process or as “value-added” post-processing on commercial CMOS wafers.

Bonded SOI (BSOI) materials has been specially designed for micromachining applications to give a low stress material that is optimised for a sacrificial release process. Trench isolation is achieved by deep dry etching to the buried dielectric. These trenches may be refill to allow metallisation to reach isolated components. Structures with aspect ratios of up to 50:1 have been realised using a combination of photolithography, deposition and deep dry etching. CMOS compatibility has been demonstrated. The process is an attractive manufacturing technology. Electroforming of nickel in resist moulds formed using conventional UV photolithography has also been investigated. Some of the early limitations with this technology have been overcome by using a new resist technology, SU8. The process needs to mature further, but remains a promising candidate. Bulk HARM uses deep dry etching of a bulk silicon membrane which is defined using wet etching. Device isolation is difficult and process control complex making this the least attractive of the technologies.

1 Introduction

There is currently much interest world-wide in developing microinertial components [1], primarily for a broad range of relatively low performance applications, such as vehicle dynamic control systems. To date, standard IC fabrication technology has been the primary enabling technology for the development of micromechanical systems. Typically, polysilicon sacrificial surface micromachining (SSM) or traditional bulk micromachining (TBM) have been used to fabricate microinertial devices.

Many advantages result from using high aspect ratio micromachining (HARM) technologies that offer added flexibility in 3 dimensions. In HARM, mechanical structures and trenches are fabricated which have large depths when compared with their widths. SSM and TBM are typically limited by practical considerations to features with a maximum aspect ratio of about 5–10. Here we demonstrate aspect ratios of between 10 and 50. This high aspect reduces unwanted cross-axis coupling, may increase capacitance in electrostatic devices, maintains high packing density as in SSM and allows thick, high mass elements to be formed for good sensitivity as in TBM – all key drivers for microinertial components in terms of performance.

For microinertial device performance to increase with the same size of device and to miniaturise the microsystem, it may be desirable to move from a hybrid solution to a fully integrated monolithic device. For this reason, we have restricted the HARM technologies discussed to CMOS compatible or potentially CMOS compatible processes with silicon as a substrate material.

2 Fabrication processes

2.1 SOI HARM

A simple, single mask process flow for SOI HARM is shown in Fig. 1. The start material is BSOI wafer. A variety of low stress, anti-stiction SOI layers and dielectric structures have been designed for micromachining applications at DERA (patent pending) and bonded by BCO Technologies. This gives a uniform 25–100 µm thick, single crystal
bonded silicon layer with a buried dielectric on a silicon handle. The thickness range was chosen as a compromise between performance, ease of processing and throughput whilst still behaving as if a bulk substrate from the point of view of CMOS circuitry.

The wafers were patterned using either a photoresist or an oxide mask and etched in a Surface Technology Systems advanced silicon etch (ASE) system [2]. This system uses the Bosch process chemistry [3] in a high density, low pressure inductively coupled plasma to etch silicon at rate of up to 2.5 μm/min with anisotropic profiles. A timed chemical etch was employed to yield suspended micromachined structures at the same time as leaving large footprint structures anchored to the substrate.

More advanced process flows include etching to preformed voids, implanting for piezoresistive pick-off, metallisation and electrically linking mechanically isolated parts. In order to make electrical contact to parts which may be mechanically isolated by deep trenches, it is necessary to provide a path for the interconnect – the quality of the refill is not critical and some voids may be tolerated without significantly degrading device performance. Rather than use a high temperature refill process, such as LPCVD nitride or polysilicon, that would degrade transistor characteristics and could not be used to post-process on commodity metallised CMOS wafers [4], we have developed a low temperature (450 °C) process based on PECVD dielectric refill at the top of trench. Metal tracks may be deposited over this bridge and patterned as interconnect – again at low temperatures. Contact is made to the desired structures by etching contact windows in the insulating dielectric layer.

2.2 UV electroforming
A potentially cheaper alternative to LIGA and SOI HARM is UV electroforming. As shown in Fig. 2, a mould is formed on a seed layer (typically copper or titanium) on wafer using conventional UV lithography. The wafer is then placed in an electroforming bath and the mould filled to the desired depth with metal (in this case, nickel). The resist is removed to leave micromechanical nickel structures. In order to produce freely suspended structures, the surface of the wafer may be patterned with a polymer sacrificial layer under the seed layer and removed at the same time as the mould.

In conjunction with Imperial College, we have investigated the use of this technology to produce electroformed nickel microinertial structures. CMOS compatibility does not necessarily result from the low temperature process as contamination and applied electric field remain issues. It should be possible to overcome this by incorporating suitable protection layers over the electronics.

2.3 Bulk HARM
TBM cannot achieve vertical sidewalls in a standard [100] silicon substrate. This leads to a reduced the packing density when compared with other HARM technologies. Special passivation layers are also needed to protect the CMOS circuitry during the wet etch. A typical bulk HARM process flow to overcome the vertical sidewall limitation is shown in Fig. 3. A membrane is defined from the back of the wafer using an anisotropic wet silicon etchant (in this case, TMAH for CMOS compatibility). Deep dry etching

![Pattern etch mask](image1)
![Deep dry etch - stopping on the buried dielectric](image2)
![Sacrificial timed etch to release structures. Large structures remain anchored](image3)

![Define a resist mould using UV lithography](image4)
![Partially fill mould in an electroforming bath](image5)
![Remove resist mould to leave nickel structures](image6)

![Pattern etch mask on the back of the wafer](image7)
![Define a membrane using a wet etch (e.g. TMAH)](image8)
![Deep dry etch to define & release structures](image9)