A high performances CMOS CCII and high frequency applications

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Abstract In this paper, we propose an improved translinear based CCII configuration. Heuristic algorithm is used for optimal sizing regarding static and dynamic performances. PSPICE simulations for AMS 0.35 μm CMOS technology show that the current and voltage bandwiths are respectively 2.6 GHz and 3.9 GHz, and the parasitic resistance at port X ($R_X$) has a value of 18 Ω for a control current of 100 μA. The improved configuration is used as a building block into high frequency design applications: a current controlled oscillator and a tunable fully integrable band pass filter. The oscillator frequency can be tuned in the range of [290–475 MHz] by a simple variation of a DC current. The central frequency of the band pass filter can be varied in the range of [1.22–1.56 GHz] and the quality factor vary in the range [8–306] with a simple variation of a DC current.

Keywords CMOS current conveyors · Optimization heuristic · Oscillators · RF band-pass filters

1. Introduction

Second generation current conveyors are one of the most well known current mode analog blocks [3]. Looking for a higher degree of control of the design characteristics, the translinear loop based configuration seems to be the most suitable configuration [1, 2]. Since their introduction, it has shown the best high frequency performances [3, 4]. However, the problem of designing a high performance integrated CCII circuit seems to be still open, especially in CMOS technology [1] where the high frequency response of current mode circuits is greatly improved. CCII based filters and oscillators present a good solution to avoid limitation of Surface Acoustic Wave filters such as problems of integration, impedance matching, tuning, linearity, etc...

In this paper, we deal with optimizing second-generation current conveyors. In order to reduce its parasitic resistance ($R_X$) at port X, we consider an improved topology of this configuration. The proposed configuration was considered for optimal sizing of the transistors. An optimizing heuristic algorithm, whose constraints are related to static and dynamic performances as well as parasitics effects, was used. To demonstrate the versatility of the optimized CCII, it was applied in different high frequency controlled circuits using voltage-mode and current-mode operations.

The paper is organized as follows: in Section 2, we present the improved translinear loop based configuration. In Section 3, we introduce the algorithmic based methodology used for optimization and present performance characteristics.
of the optimized CCII’s. In Section 4, we apply the configuration having the best performances in the design of a current controlled oscillator and a high frequency tunable band pass filter. In Section 5, we present our conclusion.

2. The proposed translinear loop based CCII configuration

The CCII is a three terminal active block. Its general representation is shown in Fig. 1. The CCII ensures two functionalities between its terminals:

– A Current follower between terminals X and Z.
– A Voltage follower between terminals X and Y.

In order to get ideal transfers, a CCII should be characterized by low impedance on terminal X and high impedance on terminals Y and Z.

Let’s focus our effort, in a first step, on lowering parasitic resistance on port XR X, by means of electronic design techniques. Let’s consider the improved CCII configuration depicted in Fig. 2 [8, 9]. In this configuration, we separate the CCII current conveying path from the signal conveying path by making a new signal path for the current transfer between ports X and Z, preserving very low impedance on port X. In that way, higher frequencies can be reached for the current conveying, since it is not done via the translinear loop. Taking into consideration the path between port X and transistors $M_7$–$M_8$ gates, the parasitic impedance $R_X$ is given by the following expression:

$$R_X = \frac{1}{g_{m8}(1 + g_{m2}r_{o2})} \frac{1}{g_{m5}(1 + g_{m4}r_{o4})}$$  \hspace{1cm} (1)

When compared to the parasitic resistance at port X of the basic translinear configuration, it is worth noting that a very good reduction is obtained [8].

The remaining parasitic resistances on ports Y and Z are respectively modelled by:

$$R_Y = \left(\frac{1}{g_{m1} + r_{o9}}\right) \left(\frac{1}{g_{m5} + r_{o14}}\right)$$  \hspace{1cm} (2)

$$R_Z = r_{o6} \left(1 - \frac{g_{m6}}{4\alpha\sqrt{\beta I_o}}\right) \left(1 - \frac{g_{m7}}{4\alpha\sqrt{\beta I_o}}\right)$$  \hspace{1cm} (3)

From the above expression, we can notice that the bias current $I_0$ directly affects the values of parasitic resistances $R_X$, $R_Z$ and $R_Y$. Although controllable parasitics can be convenient for electronic tuning of CCII based RF blocks such as filters or oscillators, their values should be limited to meet high frequency operations. Thus, we try in the followings to reduce those parasitics by optimization approach.

3. Optimization approach and simulation results

The heuristic we used for optimizing current conveyor performances is essentially a random process; it consists on the following steps [10]:

– The building of mathematical models for both constraints and preliminary conditions to satisfy. This program gives all possible quiescent parameters which are candidate for the optimisation.
– Performance criteria and error sources are mathematically modelled. These models are then taken into consideration in the program and optimal parameters can be randomly selected between the already calculated quiescent parameters.
– The optimisation approach follows the plot depicted in Fig. 3.

In fact, the Heuristic is an algorithm driven methodology which consists on minimizing X port input resistance value, maximizing Y and Z ports resistance values, maximizing high cut-off current and voltage frequencies and minimizing noise effect and silicon area. Taking into consideration these performances and error functions, the objective function $\phi$ is a weighted sum of these criteria. Since these functions have different quantity types with different range of variations,