A DLL clock generator for a high speed A/D-converter with 1 ps jitter and skew calibrator with 1 ps precision in 0.35 μm CMOS

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Abstract  This paper presents a clock generator circuit for a high-speed analog-to-digital converter (ADC). A time-interleaved ADC requires accurate clocking for the converter fingers. The target ADC has 12 interleaved fingers each running at a speed of 166 MS/s, which corresponds to an equivalent sampling frequency of 2 GS/s. A delay-locked loop (DLL) based clock generator has been proposed to provide multiple clock signals for the converter. The DLL clock generator has been implemented with a 0.35 μm SiGe BiCMOS process (only MOS-transistor were used in DLL) by Austria Micro Systems and it occupies a 0.6 mm² silicon area. The measured jitter of the DLL is around 1 ps and the delay between phases can be adjusted using 1 ps precision.

Keywords  DLL · Delay-locked loop · High speed ADC · Skew calibration

1 Introduction

Future communication systems are moving towards very high frequency digital signal processing (DSP). Today’s DSP processors have a reasonably good performance, but the problem is to provide a high performance A/D conversion with a wide input signal bandwidth. State of the art A/D converters operate around 1 GS/s with a resolution of 5 to 6 effective number of bits (ENOB) limited by the sampling jitter. However, depending on the application, the input signal bandwidth will range from 200 MHz up to 1 GHz, with a signal resolution of 8 bit, or higher, required.

The fastest available ADC architecture is the flash converter, which is capable of a sampling rate of several gigahertz with a resolution of up to 7 bits. It is assumed that the best way to meet the required specifications is to utilize time-interleaved ADC architecture. An earlier version of the clock generator was designed by using SiGe technology by AMIS [1]. During the project, this technology was closed down. In this paper, a new redesigned version of the clock generator for the ADC is presented by using a 0.35 μm SiGe process by AMS (Austria Micro Systems). The paper is organized as follows. First, the problems related to high-speed clocking and signalling are presented. The proposed new version of the clock generator based on the DLL is explained in detail and the simulation results are shown. The measurement setup and problems related to accuracy are considered. Finally, the silicon implementation and the measurement results are presented.

2 High speed clocking problems

High speed ADC’s and digital systems require an extremely clean clock signal to function properly. Phase-locked loops (PLL) and delay-locked loops (DLL) are commonly used to generate high-speed clock signals from the reference provided by an external crystal oscillator. One of the main challenges faced by modern high-speed data converters is to provide a sampling clock that has low timing errors. Jitter and skew induce errors in the clock edges used to sample the analog input signal. The skew is mainly due to component mismatch and it can be calibrated to some extent. There are two types of jitter: random and deterministic jitter which are caused by thermal or other random noise and supply variations or crosstalk, respectively.
Jitter, because of its random nature, does not create spurs at any specific frequency but degrades the signal-to-noise ratio (SNR) by raising the noise floor. The effect of sampling clock jitter can be calculated as follows

\[
\text{SNR} = 20 \log(2\pi f_{in}\sigma_a) \tag{1}
\]

where \(f_{in}\) is the frequency of sinusoid input signal and \(\sigma_a\) is standard deviated clock uncertainty. It can be seen that jitter demand for 1 GHz input frequency is strict. From Eq. (1) the conclusion can be derived that 1-GHz input frequency at 10-bit resolution results in RMS jitter less than 0.2 ps.

As the system frequency increases the jitter requirement gets more critical. Filtering the jitter from the clock signal is extremely difficult or impossible. Therefore, the performance of the external clock reference is critical when minimizing any undesired noise in the overall system. The jitter generated by a clock source can cause the A/D-converter to falsely sample the analog input signal, thus adding unwanted spectral spurs to the output and degrading the ADC’s signal-to-noise-ratio (SNR). Although PLL can reduce some of the incoming jitter from the external clock source due to its low-pass behavior, the jitter accumulation makes it more susceptible to power-supply and substrate noise. The reason DLLs are often preferred for generating clock signals is their better immunity to on-chip noise.

2.1 Jitter minimization

The amount of the jitter added to the signal has to be minimized. Each of the circuits in the signal path adds noise (jitter) to the signal, and the added jitter can not be removed. In this design the following methods have been used to minimize jitter: a low jitter external clock oscillator, simple blocks (few components/noise sources) and crosstalk minimization using separated power supply lines.

It is quite difficult to estimate or calculate the value of the added jitter. The circuit blocks have been designed in such a manner that jitter will be minimal. Some estimates for the jitter have been simulated, but due to limitations on modelling the noise, the actual jitter of the system can be acquired only by measuring the DLL. The measured results of the processed test structures can be used to optimize the jitter performance of the final clock generator.

2.2 Skew minimization

The skew between signal lines is mainly caused by the mismatch between the parameters of the components. In addition to real components, the signalling between blocks is critical, when an extremely high performance is required. The symmetry or matching between signals is essential, when equal parasitic capacitance and resistance for each signal are required. The dummy element placement and skew calibration are utilized at output phases. The vendor of the used IC-technology does not provide any statistical parameters for the target technology. Some measurements relating to parameter matching were presented in the documentation of the process vendor and it was seen that the matching is greatly improved when the transistors are non-minimum size. Throughout this design process, values as large as possible for the transistor have been utilized.

3 DLL clock generator topology

Delay-locked loops (DLL) and their applications have been widely studied during the last years. DLL-based clock multipliers and phase generators that give a very good performance have been published [2–4]. In theory a DLL could have as many delay stages as required to generate different phases. However, a large number of the delay elements increase the power consumption. The power consumption can be reduced by using a combined DLL and clock divider strategy.

A standard DLL that has delay stages, a phase comparator, charge pump and voltage regulator is shown in Fig. 1. The operation of the DLL is as follows. A clock signal CLK\(_{IN}\) is