Detection and Evaluation of Deterministic Jitter Causes in CP-PLL’s Due to Macro Level Faults and Pre-Detection Using Simple Methods

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Abstract. Charge-Pump Phase-locked loops are currently used in a variety of SoC signal generation applications. They ultimately determine performance of other SoC blocks, such as ADC’s, DAC’s, RF and synchronisation functions. In many situations, only simple frequency lock tests are carried out on the CP-PLL portion of a circuit, with other complex direct jitter tests being carried out indirectly at a higher system level. Although these higher level system tests must generally be carried out at some point they can be time consuming. In addition, if the PLL is designed and operating correctly the PLL system will generally have far better performance than the system it is driving. This paper investigates typical jitter output responses of CP-PLLs when subjected to selected forward path leakage faults. The evaluation platform consists of a macro level mixed signal based PLL-Model. Degradation of the PLL output is evaluated from the phase noise spectrum, jitter spectrum and sideband spur degradation. Further evaluations and analysis are supplied relating block level effects to jitter and phase noise. Investigations are made as to the efficacy of detection of these errors with simple measurement techniques. The crux of the work is thus initially to develop techniques to aid evaluation of the likely jitter performance of a CP-PLL system without resorting to direct measurement techniques.

Keywords: PLL, CP-PLL, jitter, deterministic jitter

1. Introduction

CP-PLLs (Charge-Pump Phase-locked loops) are currently used in a variety of situations, including on chip clock synthesis, RF (Radio Frequency) carrier synthesis, and modulation and demodulation applications. Due to the usefulness of the device, CP-PLLs [3, 13, 15, 33] are now commonplace inclusions in SoC (System on Chip) designs, and often ultimately determine performance of other SoC blocks, such as ADC’s, DAC’s, and communications channels. CP-PLLs are often evaluated in the design and characterisation phase of product development in terms of the transient response and transfer function response. Results from these evaluations will give an indication of the expected performance of the PLL (Phase-locked loop) in terms of phase noise output (or jitter output). In addition to the typical response measurements, direct jitter and phase noise measurements generally accompany design characterisation in both the simulated and real environments. In the production test phase, often it is assumed that the PLL performance is “right by design” or “guaranteed by design” and that the intrinsic noise filtering characteristics of the PLL will ensure a device with adequate performance. Examples of typical PLL analysis procedures can be found in [3, 4, 22]. The “right by design” assumption is valid for a perfect design with component variations within the process limits, however it does not hold in the presence of faults. During the design phase much effort goes into minimising the effect of noise.
introduced into the loop from external sources and maximising the natural noise suppression of the loop. Typical design methods for PLL noise suppression relate to low noise oscillator design, maximizing the loop bandwidth and efficient supply decoupling methods for the whole PLL and VCO (Voltage Controlled Oscillator). VCO’s can be very sensitive to external coupled noise from supply rails or via the substrate and these coupling mechanisms can lead to direct modulation of the VCO output signal. In many instances PLL cores situated on-chip have their own separate power supply lines and utilise techniques such as local on-chip decoupling capacitors and bond wire LC filters to desensitize the loop components to externally induced noise [19, 24, 25, 29].

As mentioned, extensive characterisation is generally used in the design and development phase of the PLL prior to production. However, tests on the PLL are usually radically reduced in the production test environment. Test reduction can occur due to many factors such as test time, access problems, and test integration. Some key issues are outlined in [5].

In many situations, only simple frequency lock tests are carried out on the PLL portion of a circuit, with other complex direct jitter tests being indirectly carried out at a higher system level. In the frequency lock test the PLL systems output signal frequency is simply measured a certain time after start-up (or after a defined change in input frequency) to see if it is at the correct operating frequency or phase. As frequency counting performs an averaging operation, it can be difficult to monitor short-term variations in the output signal. In fact it is shown in [6] and later in this paper that in many instances the PLL will still have the same average output frequency for output signals with vastly differing short-term instantaneous frequency deviations.

Indirect measurements are often carried out at the higher system level and will depend upon the final system application. These may include measurements of ADC noise (where the ADC is clocked by the PLL) or symbol synchronisation measurements (such as eye diagram measurements) of a data stream that is ultimately dependant on the PLL clock. Although these higher level system tests must be carried out at some point (unless the system is found to fail a-priori) they can be time consuming. Furthermore, test development is related to the final system function and not that of the underlying CP-PLL system. In addition, if the PLL is operating correctly and the “right by design” assumption is made, the PLL system can have a far better system performance than the system it is driving. For example jitter due to ISI (Inter Symbol Interference) in a communication channel could mask any jitter present from a correctly designed and error free PLL system. If however, the PLL system is faulty the reduced performance will propagate to the higher-level system function performance, thus leading to system degradation.

Typical faults in the CP-PLL may include charge-pump errors, loop filter errors, oscillator sensitivity to coupling noise and mismatched phase frequency detector paths [3, 10, 28, 34, 36]. Many of these errors can be highlighted using simple digital measurement techniques [6] and it seems sensible to carry out this type of test prior to more elaborate higher-level system function tests. One focus of this work is thus to attempt to rapidly isolate faulty components before investing time in more complex and time-consuming tests. The primary goal is to relate the simple open loop tests back to expected closed loop jitter or phase noise performance.

In addition, further work is being carried out to combine the results from CP-PLL forward path deviation measurements with sensitized oscillator power supply rejection ratio tests.

The primary focus of this paper is towards jitter relationships and phase noise spectrum degradation due to loop filter leakage from the main loop filter capacitor. Other forward path effects are considered briefly. This component is initially chosen because of potential sensitivity to process defects and its critical functionality in PLL operation. In embedded applications, the loop filter component is constructed from a very large (approx 100 pF) MOS capacitor structure. Also, leakage due to this component can cause analogous affects to excessive charge-pump mismatches or forward path delay faults. However, the magnitude and likelihood of performance degradation due to typical errors in the loop filter capacitor will generally be much greater. Effects from forward path errors can be highlighted using simple techniques [6]. Also, if required, contributions due to various effects can be decomposed using techniques shown in [6] and also mentioned later in this paper.

It must be mentioned at this stage that various excellent papers also exist relating to BIST (Built In Self Test), DfT (Design for Test) techniques for evaluation of various PLL parameters [2, 20, 21, 38, 41, 42]. In addition, various papers are in existence concerning behavioural modelling techniques and fault evaluation techniques for CP-PLL’s [14, 23, 26, 30, 43].