Embedded System Level Self-Test for Mixed-Signal IO Verification

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Abstract. This article presents an embedded system level self-test implementation for verification of a peripheral and its connectivity to the system. The self-test enables to perform a test for verifying the IO connectivity from inside the system. The proposed on-chip-testing scheme exploits IC level CMOS testability structures. The IC level DFT structure is verified. The scheme is confirmed by minor silicon overhead. The system level methodology is applied for a peripheral test. The methodology is evaluated by analyzing the response signal and by making a histogram data analysis. The applicability of the methodology is evaluated by comparing it to the existing methods. The article will define the approach, will list the main benefits of this methodology, analyze the laboratory test results and show the changes that need to be implemented in a mixed-signal IC in order to achieve this system level testability.

Keywords: self-test, system level, DFT, testability, IO connectivity, mixed-signal, histogram

1. Introduction

Electronic products such as mobiles contain a large number of analogue clusters in its system with the interfaces to external devices. Most of these clusters consist of drivers to external interfaces, which enable the connection to external components. The interfaces have to be verified in system tests by checking the existence of the components, the connection between the cluster and the external components. That is, it is need of IO connectivity testing. The connection is the soldered pins and wiring between the cluster and the components. The clusters themselves are amplifying, filtering, and adjusting levels, providing ESD protection, which is used between connector pins and analogue IC (integrated circuit) cluster itself. The external components are e.g., a microphone, an earpiece, a vibra element or a capacitor or external EMC components. For many products analogue clusters and their connectivity outwards are tested by functional tests. The pin test access is equipped with external pads on the printed-wired board (PWB) in order to apply test nails. The pads need an extra area on the PWB, which is a drawback in today’s products or is not anymore possible. Functional tests on the other hand are hard to generate with sufficient and known coverage and suffer from poor diagnostics.

To decrease design and test costs of a PWB a reduction of test pads is mandatory. A set of publications has addressed limited test access in analogue clusters. One of the issues is the detection and diagnosis limitation due to device tolerances. Many of these methods are based on 1149.4 standard [1]. In [2] a limited access test method, targeted at using 1149.4 is described, also presence of device tolerances. It aims at achieving good diagnostic capabilities by selecting the best nodes for measurements. In [3] a method is presented to optimise tests with restricted access. This is applied to clusters without active components and is able to be used with multiple nodes for measurements. The clusters that are discussed in this article can be connected to active components. Various publications on 1149.4 describe the features and specifications of IC implementations like [5] and [6] and describe component characterization [4] or advanced on-chip test methods on 1149.4 [7].

Apart from standardized method extensions with special cells have been proposed, targeting at detection of interconnection defects [8–11]. Implementations of these solutions generally cause less expense than 1149.4 solutions. They are not standardized and targeted a specific connection test, which makes them less suitable to test the connections of an analogue cluster. In tester perspective these solutions apply for in-house testers.
In this article it’s presented a method, which covers very well the test access mechanism to connections of an analogue cluster and its external components. It presents an applied method for verifying the presence of the components, the orientation of the component and the connectivity outside. The key factors are the minimised test-land causing minor extra silicon cost and the re-use of test methods, which are implanted as self-tests for system level verification. This method decreases the need of external test equipment by supporting introduction of self-test methods.

This article is organised as follows: the background of the methodology is presented in chapter 2. Chapter 3 introduces the embedded self-test method. In chapter 4 the implementation is discussed. In this chapter the results of the implemented DFT silicon are presented and how the method is fitted into the production. An application case of the method is discussed. Chapter 5 concludes the article.

2. Definition of Methodology

2.1. Scope of the Method

The article relates to a method and an arrangement of testing a peripheral device like an earpiece or a vibra